



## 저작자표시-비영리-변경금지 2.0 대한민국

이용자는 아래의 조건을 따르는 경우에 한하여 자유롭게

- 이 저작물을 복제, 배포, 전송, 전시, 공연 및 방송할 수 있습니다.

다음과 같은 조건을 따라야 합니다:



저작자표시. 귀하는 원저작자를 표시하여야 합니다.



비영리. 귀하는 이 저작물을 영리 목적으로 이용할 수 없습니다.



변경금지. 귀하는 이 저작물을 개작, 변형 또는 가공할 수 없습니다.

- 귀하는, 이 저작물의 재이용이나 배포의 경우, 이 저작물에 적용된 이용허락조건을 명확하게 나타내어야 합니다.
- 저작권자로부터 별도의 허가를 받으면 이러한 조건들은 적용되지 않습니다.

저작권법에 따른 이용자의 권리는 위의 내용에 의하여 영향을 받지 않습니다.

이것은 [이용허락규약\(Legal Code\)](#)을 이해하기 쉽게 요약한 것입니다.

[Disclaimer](#)

**Ph.D. DISSERTATION**

**Evaluation of deposited silicon oxide  
with post-deposition annealing for  
gate oxide of MOS capacitors on 4H-SiC**

**by**

**Suhyeong Lee**

**February 2018**

**Department of Materials Science and Engineering**

**College of Engineering**

**Seoul National University**

# **Evaluation of deposited silicon oxide with post-deposition annealing for gate oxide of MOS capacitors on 4H-SiC**

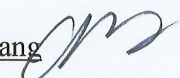
Advisor : Prof. Hyeong Joon Kim

by  
Suhyeong Lee

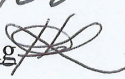
A thesis submitted to the Graduate Faculty of Seoul National  
University in partial fulfillment of the requirements for the  
Degree of Doctor of Philosophy  
Department of Materials Science and Engineering


February 2018

Approved by

Chairman of Advisory Committee : Cheol Seong Hwang 

Vice-chairman of Advisory Committee : Hyeong Joon Kim 

Advisory Committee : Seong-Hyeon Hong 

Advisory Committee : Jeong Hyun Moon 

Advisory Committee : Min-Woo Ha 

# Abstract

Silicon carbide (SiC) is one of the promising materials being developed for the application of power devices. The 4H-SiC metal-oxide-semiconductor field effect transistors (MOSFETs) using 4H-SiC as substrate are expected to play a major role as a power semiconductor device. However, carbon clusters, which are formed in the oxidation process, increase interface states, and thus deteriorate device performance. Many researches have reported that the efficient method to remove the interfacial traps is the post-oxidation annealing (POA) using nitric oxide (NO) gas, which has become common process to remove interface traps. Although NO POA is effective on reducing interface traps, it is necessary to find the alternative and advanced methods to reduce interface traps effectively: deposition is one of them, because the most of carbon clusters are formed during oxidation process. The deposition of oxide films has been usually carried out by chemical vapor deposition (CVD) and atomic layer deposition (ALD). ALD oxide with NO post-deposition annealing (PDA) showed excellent performance was reported, but the MOSFET, which was fabricated with the ALD oxide, consisted of thin oxide less than 30 nm. However, the commercial products commonly used thicker than 50 nm. In this dissertation, oxide films thicker than 40 nm were deposited by ALD or sputtering, and then MOS capacitors were fabricated to evaluate their electrical and physical properties. And the effects of PDA conditions on the deposited oxide were also investigated. In addition, to evaluate the feasibility of oxide deposition without PDA, the oxides, which were deposited on the thermal

buffer oxide, were also investigated.

In order to densify the 50 nm SiO<sub>2</sub> oxide film deposited with plasma-enhanced ALD (PEALD), the PDA was performed using Ar gas, which is an inert gas. At this time, the PDA was operated at 400, 600, 800, 1000, and 1200°C for 2 h. HF etch test and leakage current analysis showed that the oxide film was stabilized after densifying at 1000°C or higher. However, in the capacitance–voltage (*C–V*) characteristics, the densified sample at 1000°C was found to be in a less stable state, but a stable oxide film was formed only at 1200°C. In addition, the NO PDA, known to be effective at 30 nm, was conducted for 2 h at 1200°C on PEALD oxide. The *C–V* hysteresis decreased significantly compared to the as-dep oxide, but the flat-band voltage (*V<sub>FB</sub>*) shifted significantly in the negative direction. This is because the thicker the oxide film, the greater the positive charging by nitrogen atoms.

On the other hand, sputtering is a traditional physical vapor deposition (PVD) method, but it has not been often used to deposit the gate insulating films. To evaluate whether this sputtering SiO<sub>2</sub> oxide film can be used as an insulating film, MOS capacitors with sputtered oxide were fabricated and their electrical properties and physical properties were also analyzed. N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA were conducted to stabilize the sputtered oxide. All the samples were found to be sufficiently densified through refractive index measurement and HF etching test, and in the case of O<sub>2</sub> PDA, an additional oxidation reaction occurred. As a result of the insulation property evaluation, N<sub>2</sub> and NH<sub>3</sub> did not have good insulation characteristics, which seems to be the result of the chemical reaction of nitrogen, increasing the leakage current. In the case of O<sub>2</sub> and NO, they showed insulation characteristics but it was insufficient compared

to thermal oxide. For the optimization of NO PDA for sputtering oxide, the 30, 60, and 90 min of NO PDAs were also investigated. As PDA time increased,  $V_{FB}$  was negatively shifted and hysteresis decreased. As a result of normalized conductance–frequency ( $G_p-\omega$ ) and  $D_{it}$  characteristics, the lowest interface traps were shown in the 60 min NO PDA among three conditions.

Since both PEALD and sputtering use plasma, it is necessary to judge whether the plasma damage affects the substrate and interface characteristics. A passivation layer was formed through pre-oxidation before deposition, and then an oxide film was formed through PEALD and sputtering. As-deposition oxide without PDA showed poor insulating properties and large leakage current. However, pre-oxidation greatly reduced the leakage current and allowed a normal  $C-V$  curve to be obtained. Although the leakage current is not as good as that of the thermal oxide, the overall characteristics are sufficiently improved for both PEALD and sputtering oxide. Based on these results, pre-oxidations using NO and  $N_2O$  were conducted, and showed superior  $C-V$  characteristics when using  $N_2O$  and NO/ $O_2$  mixed gas.

In this dissertation, whether the deposition  $SiO_2$  can be used as the gate oxide was investigated. To improve characteristics of PEALD and sputtering  $SiO_2$ , post-deposition annealing and pre-oxidation were conducted. The applicability of PEALD and sputtering oxide was investigated through PDA and pre-oxidation under various conditions. If the deposition and annealing conditions were optimized, deposition oxide will have competitive enough to be used as a gate oxide for 4H-SiC MOS device.

---

**Keywords:** 4H-SiC, MOS capacitor, PEALD, sputtering, post-deposition annealing

**Student Number:** 2011-20658

# Contents

<b>Abstract .....</b>	<b>i</b>
<b>Contents .....</b>	<b>v</b>
<b>LIST OF TABLES .....</b>	<b>ix</b>
<b>LIST OF FIGURES .....</b>	<b>x</b>
<b>Chapter 1. Introduction .....</b>	<b>1</b>
1.1 SiC Power Device .....	1
1.1.1 Power device .....	1
1.1.2 Conventional MOS Device .....	5
1.1.3 Application of SiC for power device and SiC MOS device .....	7
1.2. Material Properties of SiC .....	9
1.2.1 Structural properties .....	9
1.2.2 Thermal properties .....	12
1.2.3 Optical properties .....	14
1.2.4 Electrical properties .....	16
1.3 Gate Oxide Issue for SiC MOS Device .....	20
1.3.1 Conventional SiC MOSFET .....	20
1.3.2 The formation of defect between SiO <sub>2</sub> /SiC interface .....	23
<b>Chapter 2. Literature Review .....</b>	<b>27</b>
2.1 Fabrication Method of Gate Oxide .....	27
2.1.1 Thermal oxide on SiC .....	27
2.1.2 CVD oxide .....	31



2.1.3 ALD oxide .....	33
2.1.4 PVD oxide .....	35
2.2 Nitridation of SiO <sub>2</sub> on SiC for MOS device .....	37
2.2.1 NO and N <sub>2</sub> O post-oxidation annealing .....	39
2.2.2 N <sub>2</sub> post-oxidation annealing.....	43
2.2.3 Other nitridation methods .....	45
2.3 Basic of Device Measurement .....	49
2.3.1 C–V measurement.....	49
2.3.2 Interface state density measurement .....	54
2.3.3 J–E measurement.....	58
2.4 Electrical Characteristics of Gate Oxide on SiC.....	60
2.4.1 Thermal oxide .....	60
2.4.2 CVD oxide .....	63
2.4.3 ALD oxide .....	67
2.4.4 PVD oxide .....	73
<b>Chapter 3. Experiment and Analysis .....</b>	<b>78</b>
3.1 Sample Preparations .....	78
3.1.1 4H-SiC wafer information .....	78
3.1.2 Wafer cleaning process .....	78
3.2 Gate Oxide Deposition and Oxidation.....	79
3.2.1 Plasma-enhanced atomic layer deposition system.....	79
3.2.2 PEALD conditions of gate oxide deposition .....	80
3.2.3 Sputtering system and deposition condition .....	82

3.2.4 Dry oxidation process .....	83
3.3 Post-deposition annealing process .....	85
3.3.1 Apparatus of furnace for PDA .....	85
3.3.2 Ar post-deposition annealing .....	85
3.3.3 NO post-deposition annealing .....	86
3.3.4 N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> Post-deposition annealing.....	86
3.4 MOS Capacitor Fabrication .....	88
3.5 Measurement and Analysis .....	89
3.5.1 Physical and chemical analysis of gate oxide .....	89
3.5.2 Electrical properties measurement of MOS capacitor .....	90
<b>Chapter 4. Results and Discussions.....</b>	<b>92</b>
4.1 Characteristics of PEALD Oxide with PDA.....	92
4.1.1 Effects of Ar PDA.....	92
4.1.2 Effects of NO PDA on 50nm SiO <sub>2</sub> .....	99
4.2 Characterisitics of Sputtered Oxide with PDA .....	102
4.2.1 Physical and chemical properties.....	102
4.2.2 <i>J-E</i> and oxide breakdown characteristics .....	108
4.2.3 <i>C-V</i> and D <sub>it</sub> characteristics.....	111
4.3 Analysis of Sputtered Oxide with NO PDA .....	117
4.3.1 <i>C-V</i> curve analysis .....	117
4.3.2 Modeling of charging in near interface traps .....	121
4.3.3 <i>G-ω</i> and D <sub>it</sub> analysis.....	124
4.4 Deposited Oxide with Thermal Oxide Interlayer.....	127

4.4.1 PEALD oxide with dry thermal oxide .....	127
4.4.2 PEALD oxide with NO thermal oxide.....	132
4.4.3 PEALD oxide with NO/O <sub>2</sub> and N <sub>2</sub> O thermal oxide.....	135
4.4.4 Sputtering Oxide with dry thermal oxide .....	140
4.5 Experiments Summary .....	144
<b>Chapter 5. Conclusions .....</b>	<b>146</b>
<b>CURRICULUM VITAE.....</b>	<b>148</b>
<b>REFERENCES .....</b>	<b>154</b>
<b>LIST OF PUBLICATIONS.....</b>	<b>163</b>
국문 초록 .....	171
감사의 글 .....	174

# LIST OF TABLES

Table 1.1. Thermal conductivity, thermal expansion coefficient, and decomposition temperature of SiC polytypes. ....	13
Table 1.2. Hexagonality, optical band gaps, and exciton energy gap of various SiC polytypes. [13, 14].....	15
Table 1.3. The electrical properties of 3C-SiC, 4H-SiC, 6H-SiC, Si, GaAs, and GaN .....	18
Table 1.4. The figure of merits for various semiconductors. [15-18].....	19
Table 4.1. Thickness and refractive index at 632.8 nm of the SiO <sub>2</sub> on 4H-SiC before and after N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> , and NO PDA.....	105
Table 4.2. Measured flat-band voltage ( $V_{FB}$ ), $C-V$ hysteresis ( $\Delta V_{hys}$ ), and effective oxide charge density ( $Q_{eff}$ ) extracted from $C-V$ . The “L” means left curve and “R” means right curve.....	120
Table 4.3. Capacitance equivalent thickness (CET) and real oxide thickness ( $t_{ox}$ ) of dry oxidation oxide and pre-oxidized/PEALD oxide. ....	129
Table 4.4. Capacitance equivalent thickness (CET) and real oxide thickness ( $t_{ox}$ ) of dry oxidation oxide and pre-oxidized/PEALD oxide. ....	142

# LIST OF FIGURES

Figure 1.1. The usage of life-related power device. [2] .....	3
Figure 1.2. A schematic diagram of the role of power devices. ....	3
Figure 1.3. The prediction of SiC device sales by applications. (Published in Yole Développement in 2014).....	4
Figure 1.4. A schematic view of a classical bulk n-channel MOSFET. [3].....	6
Figure 1.5. Simplified device cross section of the 4H-SiC power BJT. [4] .....	8
Figure 1.6. Cross-sectional view of 4H-SiC MESFET design utilizing epitaxially grown $N^+$ source and drain mesas. [5].....	8
Figure 1.7. The characteristic tetrahedron building block of all SiC crystals. Four carbon atoms are covalently bonded with a silicon atom in the center. Two types exist. One is rotated $180^\circ$ around the c-axis with respect to the other, as shown. [6] .....	11
Figure 1.8. The three most common polytypes in SiC viewed in the [1120] plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; k and h denote crystal symmetry points that are cubic and hexagonal, respectively. [6] .....	11
Figure 1.9. The D-MOSFET structure. [19].....	22
Figure 1.10. Power D-MOSFET structure with its internal resistances. [19]	22
Figure 1.11. Comparison of interface state density at the SiO <sub>2</sub> /SiC interface of different SiC polytypes and at the SiO <sub>2</sub> /Si interface reduced by hydrogenation. [23] .....	25
Figure 1.12. Schematic overview of the experimental data on the $D_{it}$ (E) at the 4H-SiC/SiO <sub>2</sub> interface (top) and the carbon cluster model for	

explanation of the $D_{it}$ (E) (bottom). [24] .....	26
Figure 2.1. Oxide growth rates as a function of oxide thicknesses at various temperatures for the (0001) Si- (green triangles), the (1120) a- (blue squares), the (1100) m- (red diamonds), and the (0001) C-face (orange circles) of 4H-SiC dry thermal oxidation. [32] .....	29
Figure 2.2. Schematic diagrams of Si–C bonds on the SiC surface. The orange arrow denotes Si back-bond. [33] .....	30
Figure 2.3. Reaction principle and steps of CVD. [34] .....	32
Figure 2.4. 4 step of ALD: 1) source pulse, 2) source purge, 3) reactant pulse, 4) reactant purge. [36] .....	34
Figure 2.5. Schematics of simplified sputtering system: (a) DC, (b) RF. ....	36
Figure 2.6. The schematic diagram of nitridation. [39] .....	38
Figure 2.7. Interface state density versus gate voltage for MOS capacitors with.....	41
Figure 2.8. Typical normalized HF $C-V$ curves of both NO and $N_2O$ annealed/grown oxides and Ar annealed oxides. [42] .....	41
Figure 2.9. Nitrogen SIMS profiles through NO nitrided (black triangle), NO grown (dotted line), $N_2O$ nitrided (white circle), and $N_2O$ grown (line) oxides grown on 4H SiC. [42] (The depth scale was established from the sputtering rate, calculated from the sputtering time corresponding to 50% of oxygen intensity—labeled as “0 nm”; the oxide thickness was measured from the accumulation capacitance of corresponding MOS capacitor.) .....	42
Figure 2.10. (a) Energy levels for interstitial C and C clusters in SiC. (b) C	

and .....	42
Figure 2.11. Change in the N 1s core-level spectra obtained from the N <sub>2</sub> -POA treated SiC samples with 15-nm-thick thermal SiO <sub>2</sub> layers after complete SiO <sub>2</sub> removal. The POA in pure N <sub>2</sub> ambient was done for 30 min at different temperatures, i.e. 1400°C (upward red triangles), 1350°C (downward blue triangles), and 1300°C (green rhombuses). The as-oxidized SiO <sub>2</sub> /SiC sample without post annealing (black filled squares: as-ox.) is also shown for comparison. Peak intensity was normalized by the Si 2p peak intensities (not shown). [44] .....	44
Figure 2.12. Relationship between D <sub>it</sub> measured for each process and energy from conduction band between 0.2 eV and 0.6 eV. The D <sub>it</sub> measured at 0.2 eV steadily decreases as the nitrogen plasma POA time increases. [45] .....	47
Figure 2.13. XPS profile of the N 1s nitrogen at the SiO <sub>2</sub> /SiC interface after oxide etch. [45].....	47
Figure 2.14. Correlation graphs of extracted peak of species intensity values from SIMS characterization for all samples. (a) Carbon intensity and CN <sup>-</sup> intensity, (b) Si <sup>-</sup> intensity and SiN <sup>-</sup> intensity. [47].....	48
Figure 2.15. Energy-band diagrams of an ideal MOS (MIS) capacitor with a p-type semiconductor at V <sub>G</sub> = 0 for (a) accumulation, (b) depletion, and (c) inversion conditions. [48] .....	51
Figure 2.16. MIS <i>capacitance–voltage</i> characteristics under (a) low-frequency, (b) high-frequency, and (c) deep-depletion conditions. [50] .....	52
Figure 2.17. Effect of a fixed charge Q <sub>f</sub> on a MIS capacitor with an n-type	

semiconductor (left), [51] and the resulting parallel shifts of the $C-V$ curves relative to ideal ones for a p-type semiconductor (right). [49]	52
Figure 2.18. Stretchout in $C-V$ curves due to interface-state charge $Q_{it}$ . [49]	53
Figure 2.19. High- and low-frequency $C-V_G$ curves showing the offset $\Delta C/C_{ox}$ due to interface traps. [52].....	57
Figure 2.20. Equivalent circuits for conductance measurements; (a) MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$ , (b) simplified circuit of (a), (c) measured circuit, (d) circuits including series resistance ( $r_s$ ) and tunneling conductivity ( $G_t$ ).....	57
Figure 2.21. Typical conduction processes in insulators along with their expressions and illustrations (h: Planck's constant, $m^*$ : Effective mass of an electron). [49].....	59
Figure 2.22. Oxide current density as a function of field for an n-type 6H-SiC sample at 140°C. Oxide thickness is 20.5 nm. [57] .....	62
Figure 2.23. Schematic energy-band diagrams of a MOS structure. The numbering (1) – (4) refers to respective leakage paths due to Schottky emission, Poole-Frenkel emission, Fowler-Nordheim tunneling, and direct tunneling. $E_C$ , $E_F$ , $E_V$ , and $E_{FM}$ are the conduction band edge, Fermi level, valence band edge, and Fermi level of Ni, respectively. [59] .....	62
Figure 2.24. (a) $C-V$ characteristics and (b) extracted $V_{FB}$ and $Q_{eff}$ of SiC MOS capacitor with different annealing temperature. Gate oxide of capacitors deposited by LPCVD using $SiH_4$ and $O_2$ at 400°C. [60]...	65
Figure 2.25. $D_{it}$ of SiC MOS capacitors using CVD oxide and thermal oxide with NO PDA. HTO, LTO, and reox mean HTCVD oxide, LTCVD	



oxide, and re-oxidation ( $N_2$ , 1h, $950^\circ C$ ), respectively. [61] .....	65
Figure 2.26. Effect of annealing ambients and interfacial oxidation on the interface states density for 4H-SiC MOS capacitors. [62] .....	66
Figure 2.27. Comparison of the field-effect electron channel mobility in transistors with gate made with standard dry oxidation ( $1150^\circ C$ 3 h, $O_2+Ar+950^\circ C$ Wet Reox), and with 10 nm dry oxide ( $1050^\circ C$ 1 h, $O_2$ ) and $SiO_2$ -TEOS annealed in Ar. [62].....	66
Figure 2.28. $C-V$ characteristics of MOS capacitors with (a) thermally grown oxides and (b) ALD oxides as a function of NO POA duration. [65] 70	
Figure 2.29. $D_{it}$ distributions as a function of energy level. [65] .....	71
Figure 2.30. $\mu_{FE}$ of MOSFETs using thermally grown oxide only, thermally grown oxide with 120 min NO POA, and ALD oxide with 180 min NO POA. [65] .....	71
Figure 2.31. 1 M, 100 k, and 10 k-Hz $C-V$ characteristics of MOS capacitors .....	72
Figure 2.32. Selectively etched $SiO_2$ layer grown on Si-face SiC substrates by wet thermal oxide process. [69] .....	75
Figure 2.33. Selectively etched $SiO_2$ layer, which is grown on Si-face 4H-SiC substrate by sputtering. [69] .....	75
Figure 2.34. Si 2p photoelectron spectra (a.u. stands for arbitrary units) at a take-off angle sensitive to the surface of Si-faced 4H-SiC samples thermally nitrided in 30 mbar of $^{15}NH_3$ for 1 h at different temperatures, as indicated. [70].....	76
Figure 2.35. $I-V$ curves of Al/ $SiO_2$ /(nitrided) 4H-SiC structures obtained from 4H-SiC samples submitted to 30 mbar of $^{15}NH_3$ for 1 h at $900^\circ C$ .	

(solid symbols) and 1100°C (open symbols) followed by deposition of a 20-nm oxide film by sputtering and addition of Al and GaN contacts. Indicated samples were submitted to PDA in 400 mbar of Ar for 1 h at indicated temperatures. Results from a SiO<sub>2</sub> film formed by SiC thermal oxidation submitted to PDA at 1000°C are also presented for comparison. [70]..... 77

Figure 3.1. A schematic diagram of plasma-enhanced ALD system used in experiment..... 81

Figure 3.2. Molecular structure of BDEAS precursor..... 81

Figure 3.3. A schematic diagram of the sputtering system..... 84

Figure 3.4. Steps of dry oxidation for thermal oxide on 4H-SiC. .... 84

Figure 3.5. A schematic diagram of the furnace system..... 87

Figure 4.1. Etched thickness of PEALD oxide without and with PDA. Thermal oxide was also etched as reference. .... 96

Figure 4.2. AFM images of 4H-SiC surface after SiO<sub>2</sub> etching by diluted HF. The initial surfaces were (a) bare substrate, (b) thermal oxidized SiO<sub>2</sub>, PEALD SiO<sub>2</sub> (c) without and with Ar PDA at (d) 400, (e) 600, (f) 800, (g) 1000, (h) 1200°C, respectively. .... 96

Figure 4.3. *J–E* characteristics of PEALD oxide (a) without PDA and with Ar PDA at (b) 400 (c) 600, (d) 800, (e) 1000, and (f) 1200°C, respectively. Each measurement was conducted at 25, 45, 65, 85, 105, and 125°C, respectively..... 97

Figure 4.4. *C–V* and *G–V* characteristics of PEALD oxide with Ar PDA at (a)

400, (b) 600, (c) 800, (d) 1000, and (e) 1200°C.....	98
Figure 4.5. $C-V$ characteristics of MOS capacitors with 50 nm-deposited SiO <sub>2</sub> . The PDA was operated at 1175°C for 2 h using NO gas. ....	101
Figure 4.6. Auger electron spectroscopy (AES) results of ALD oxide with NO PDA.....	101
Figure 4.7. Etching rate of the SiO <sub>2</sub> on 4H-SiC before and after N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> , and NO PDA by dilute HF.....	106
Figure 4.8. (a) Si 2p and (b) N 1s XPS spectra of the SiO <sub>2</sub> /4H-SiC after N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> and NO PDA. ....	107
Figure 4.9. Gate leakage current density of the SiO <sub>2</sub> /4H-SiC MOS capacitors using N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> and NO PDA. ....	110
Figure 4.10. Breakdown field of the SiO <sub>2</sub> /4H-SiC MOS capacitors using N <sub>2</sub> , NH <sub>3</sub> , O <sub>2</sub> and NO PDA. ....	110
Figure 4.11. $C-V$ characteristics of the SiO <sub>2</sub> /4H-SiC MOS after O <sub>2</sub> and NO PDA.....	114
Figure 4.12. $C-V$ characteristics of the SiO <sub>2</sub> /4H-SiC MOS after O <sub>2</sub> and NO PDA with different start voltage. The arrow indicates the start voltage. .....	115
Figure 4.13. $D_{it}$ of the SiO <sub>2</sub> /4H-SiC MOS after O <sub>2</sub> and NO PDA. For comparison, $D_{it}$ of thermal SiO <sub>2</sub> is also shown. ....	116
Figure 4.14. $C-V$ characteristics of the SiO <sub>2</sub> /4H-SiC MOS after NO PDA with various annealing time. The voltage swept from depletion (−4 V) to accumulation (6 V) and back in (a), and from accumulation to depletion and back in (b).....	119
Figure 4.15. Negative charging model at near interface traps when positive	

voltage applied. (a) Near interface traps are not charged initially. (b) In accumulation, negative charges are trapped in near interface traps. (c) $V_{FB}$ are shifted to positive by negative charging. ....	122
Figure 4.16. Initially positive charging model at near interface traps. (a) Near interface traps are positive charged initially. (b) In accumulation, positive charges are de-trapped in near interface traps. (c) $V_{FB}$ are shifted to positive voltage when compared to the initial charging state. ....	123
Figure 4.17. Normalized conductance characteristics at different energy levels ( $E_c - E_t$ ) of (a) 0.62 , (b) 0.35 and (c) 0.15 eV.....	126
Figure 4.18. $D_{it}$ distributions as a function of energy level with frequency ranges of $10^3$ to $10^6$ Hz.....	126
Figure 4.19. Normalized capacitance of dry oxidation oxide and pre-oxidized/PEALD oxide. ....	129
Figure 4.20. $C-V$ frequency dispersion characteristics of (a) 27 nm-thick dry oxide, (b) 40 nm-thick dry oxide, (c) 10 nm-thick dry oxide/30 nm-thick PEALD oxide, and (d) 20 nm-thick dry oxide/20 nm-thick PEALD oxide. ....	130
Figure 4.21. $J-E$ characteristics of (a) 27 nm-thick dry oxide, (b) 40 nm-thick dry oxide, (c) 10 nm-thick dry oxide/30 nm-thick PEALD oxide, and (d) 20 nm-thick dry oxide/20 nm-thick PEALD oxide. ....	131
Figure 4.22. $C-V$ characteristics of 8 nm-thick NO-oxidized oxide/43 nm-thick PEALD oxide and 13 nm-thick NO-oxidized oxide/38 nm-thick PEALD oxide. ....	133
Figure 4.23. TZDB characteristics of (a) 8 nm-thick NO-oxidized oxide/43	

nm-thick PEALD oxide and (b) 13 nm-thick NO-oxidized oxide/38	
nm-thick PEALD oxide.....	133
Figure 4.24. N 1s spectra of SiO <sub>2</sub> surface by XPS analysis after O <sub>2</sub> and NO	
oxidation.....	134
Figure 4.25. C–V characteristics of NO+O <sub>2</sub> -oxidized oxide/PEALD oxide. For	
comparison, O <sub>2</sub> -oxidized oxide/PEALD oxide and NO-oxidized	
oxide/PEALD oxide are also shown. ....	137
Figure 4.26. C–V characteristics of N <sub>2</sub> O-oxidized oxide/PEALD oxide. N <sub>2</sub> O	
oxidation was conducted during 30 and 60 min. High pressure sample	
was conducted N <sub>2</sub> O oxidation above 760 Torr during 30 min. ....	138
Figure 4.27. (a) Si 2p and (b) N 1s spectra of thin N <sub>2</sub> O-oxidized oxide and	
NO/O <sub>2</sub> -oxidized oxide in XPS analysis.....	138
Figure 4.28. J–E characteristics of (NO+O <sub>2</sub> )-oxidized oxide/PEALD oxide.	
For comparison, dry thermal oxide was also shown. ....	139
Figure 4.29. C–V characteristics of N <sub>2</sub> O-oxidized oxide/PEALD oxide. For	
comparison, dry thermal oxide was also shown.....	139
Figure 4.30. C–V characteristics of dry-oxidized oxide/sputtering oxide. ...	142
Figure 4.31. D <sub>it</sub> of dry thermal oxide/sputtering oxide. ....	143
Figure 4.32. J–E characteristics of dry thermal oxide/sputtering oxide. SPT	
means sputtering oxide.....	143

# **Chapter 1. Introduction**

## **1.1 SiC Power Device**

### **1.1.1 Power device**

Today, the semiconductor devices play the largest role in many aspects of modern society. Computer-based process has changed the paradigm of the industry for several decades, and the Internet and network technologies have led to an information revolution. In the last decade, smartphones and cloud systems have once again set a new milestone in the information society. Furthermore, industries that require semiconductors are still changing, and replacement of human using artificial intelligence is a prime example. As these semiconductor applications have grown, stable supply of electricity has become essential. In particular, there has been a need to improve not only the efficiency of the power generation stage but also the efficiency of the transmission stage and the standby power, and the next generation intelligent power grid called the Smart Grid is proceeding as a national business.

Power device are electrical device used at high voltage like the Smart Grid. Fig. 1.1 shows where the power device is used. Even for large-scale such as smart grids, applications such as electric vehicles, hybrid vehicles, power supplies of cloud server, and emergency power systems also require high voltage, and semiconductor devices used for these purpose are power devices. Power devices are based on the four roles shown in the Fig. 1.2. By acting as

convertor, frequency conversion device, switching regulator and inverter, The power device controls the alternation current voltage and direct current voltage.

The basis of such a semiconductor industry starts from a substrate which is made of silicon (Si). Although the material that made the first solid-state transistor is known as germanium (Ge), silicon has become an important material for the mass production of semiconductor industry because of its chemically stability, easy manufacture and numerous amounts. However, silicon technology has been steadily developed and approached its limit. Especially, in high power, high temperature and high frequency environments such as power devices, the desire for new materials has been increasing exponentially in recent years, and research on substitute materials is also increasing. Silicon Carbide (SiC) is one of the main materials being developed for the purpose of power devices. [1] The characteristics of SiC for power devices are discussed in Chap. 1.2. High melting point, high breakdown voltage and wide bandgap of SiC were sufficient to perform the role of power semiconductors, but rather difficult to manufacture due to high melting point caused high price problems. However, with a lot of research and investment in the world, 4-inch of diameter or more wafers are now on the market, and the prices are getting cheaper.

Currently, SiC is also a nationally important material in Republic of Korea and research is actively underway. Fig. 1.3, published in Yole Développement in 2014, predicts market demand for SiC. According to this, the demand for PFC and PV inverters was the majority in 2014, but in 2020, it will be used for more advanced technology such as electric/hybrid vehicle, smart grid, wind power, and motor control.

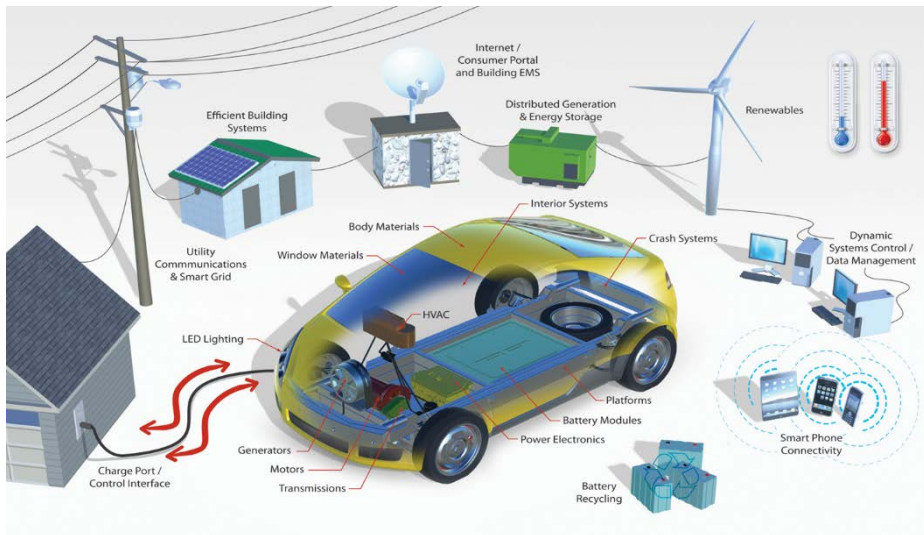


Figure 1.1. The usage of life-related power device. [2]

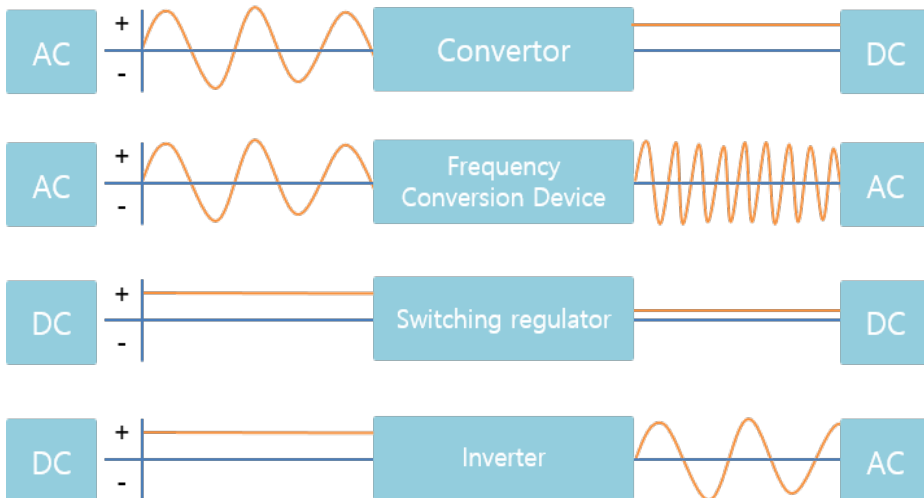


Figure 1.2. A schematic diagram of the role of power devices.



**SiC device sales in %, by applications**  
 (Source : SiC Modules, Devices and Substrates for Power Electronics Market, Yole Développement, October 2014)

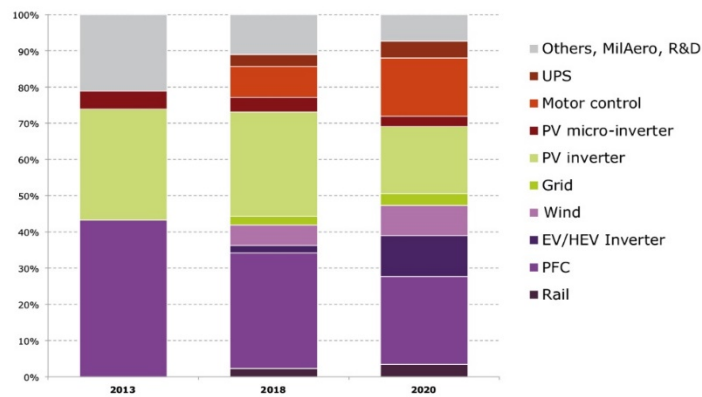


Figure 1.3. The prediction of SiC device sales by applications. (Published in Yole Développement in 2014)

### 1.1.2 Conventional MOS Device

There are many kinds of semiconductor devices, but metal-oxide-semiconductor field effect transistor (MOSFET) is the most important device of semiconductor. Basically, the rectifying and amplifying characteristics are the same as those of other transistors such as bipolar junction transistor (BJT), junction gate field effect transistor (JFET), but MOSFETs are used as devices for fabricating integrated circuit (IC) or large scale integration (LSI) because they have a simple structure and are easy to integrate.

The classical n-MOSFET is shown in the Fig. 1.4. [3] A source and drain are formed by implanting  $n^+$  ions on a p-type substrate. After implantation and ion activation annealing, an oxide film is formed by oxidation or deposition, and then a gate metal is deposited thereon. Applying a voltage to the gate creates an inversion region between the source and the drain, called the channel, and allows the current to flow between the source and drain. At this time, the gate voltage does not directly affect the channel but affects the field effect, thus acting as switching device. The substantially flowing current is the drain voltage, which can act as an amplification role by adjusting the drain voltage.

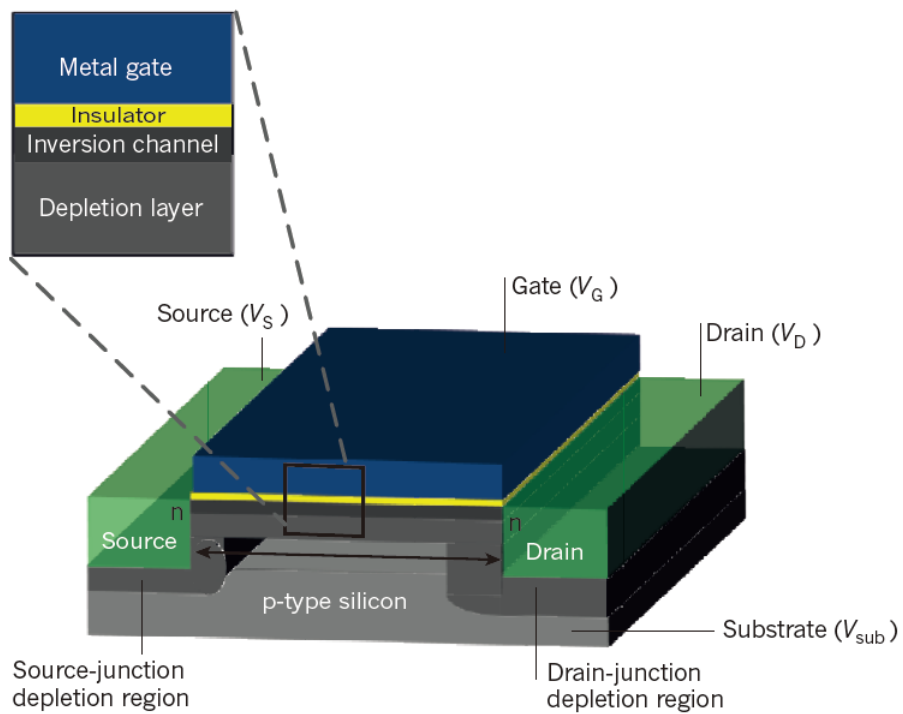


Figure 1.4. A schematic view of a classical bulk n-channel MOSFET. [3]

### 1.1.3 Application of SiC for power device and SiC MOS device

As with conventional silicon, SiC wafers can be used as substrates for various applications such as BJT (Fig. 1.5), JFET, metal-semiconductor field effect transistor (MESFET, Fig. 1.6), MOSFET and insulated gate bipolar transistor (IGBT). Among these transistors, SiC MOSFET devices have been rapidly developed and mass-produced since they are simple in structure and used as main elements of silicon process. [3] In the MOSFET, stable gate oxide formation is very important. In the conventional silicon semiconductor, silicon dioxide ( $\text{SiO}_2$ ) is formed as a gate insulating film through a thermal oxidation process. Unlike GaAs and GaN, SiC is a material that can form  $\text{SiO}_2$  through the oxidation process. Therefore, the gate oxide is formed mainly through the oxidation process from the initial SiC MOSFET to the present.

Fabrication of SiC MOSFETs includes implantation, activation annealing, oxidation, and metallization. The evaluation of the characteristics of the MOSFET can be regarded as a comprehensive reflection of all these factors. On the other hand, metal-oxide-semiconductor (MOS) capacitors can be used instead of the MOSFETs in order to concentrate the characteristics of the oxide film or the interface characteristics, and to minimize other parameters like the metallization or implantation process. The MOS capacitors can measure flat band voltage, oxide capacitance, slope, interface state density, and leakage current, which are related to the threshold and mobility characteristics of MOSFETs. In this dissertation, I will mainly deal with the characteristics of oxide films and interface defects using MOS capacitors.

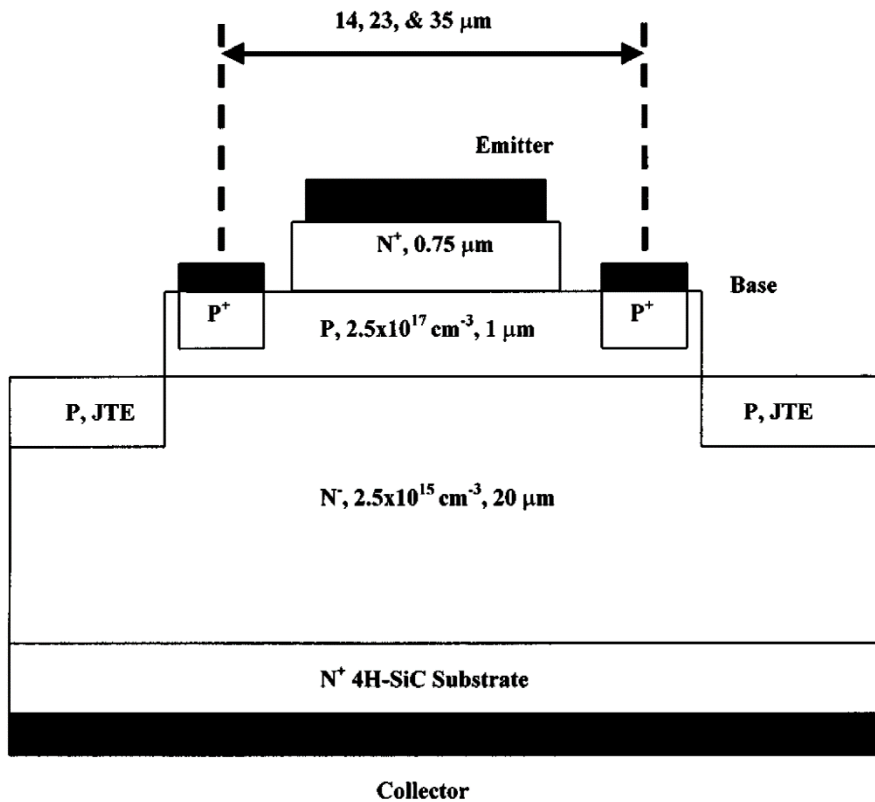


Figure 1.5. Simplified device cross section of the 4H-SiC power BJT. [4]

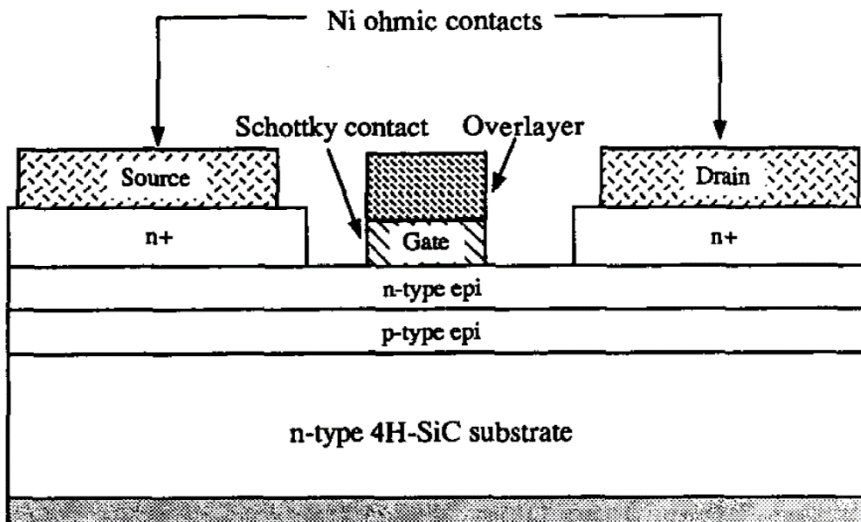


Figure 1.6. Cross-sectional view of 4H-SiC MESFET design utilizing epitaxially grown  $\text{N}^+$  source and drain mesas. [5]

## 1.2. Material Properties of SiC

As mentioned in the previous Chap. 1.1, SiC is material for high-power, and high-temperature and high-frequency environment. SiC can form a stable  $\text{SiO}_2$  oxide film, which is a great advantage over other competing materials. The industrial application of SiC began with the blue light emitting diode (LED), but now SiC also used in the power semiconductor industry. [6] SiC is a compound semiconductor, not a monatomic material, so it will be different in properties from conventional silicon. In this chapter, characteristics of SiC will be described one by one.

### 1.2.1 Structural properties

The basic structure of SiC is the tetrahedron of four carbon atoms with a silicon atom in the center. [6] That is, it is the same as the case where one Si is replaced with C in a monatomic Si structure having a diamond structure. The illustration of SiC atomic structure is shown in Fig. 1.7. [6] The Si–C bonding consists of 88% of covalent bonds and 12% of ionic bonds, [7] and the bond lengths between C–C (Si–Si) and Si–C atoms are 3.08 Å and 1.89 Å, respectively. [6]

This structure of SiC forms many polytypes. It can exist in about 130 polytypes depending on the stacking method of atoms. [8] Generally, it can be classified into zinc-blende structure or wurtzite structure according to the stacking sequence. The zinc-blende structure can be compared to cubic and the

wurtzite structure can be compared to hexagonal when it is treated as monatomic structure, so it is called cubic and hexagonal structure more. Stacking sequences refer to the order of stacking on three sites in close packing, which is divided into A, B, and C sites. The most common three types of polytypes, which are 4H-SiC, 6H-SiC, and 3C-SiC, are shown in Fig. 1.8

**Figure 1.8.** In the name of the polytypes, the number indicates repeated sequence sites, H means hexagonal, C means cubic, and R means rhombohedral. That is, 4H-SiC is sequence repetition of ABCB, 6H-SiC is ABCACB, and 4C is ABC repetition. SiC has different properties depending on the poly type. Currently, SiC used as a semiconductor device mainly uses 4H-SiC.

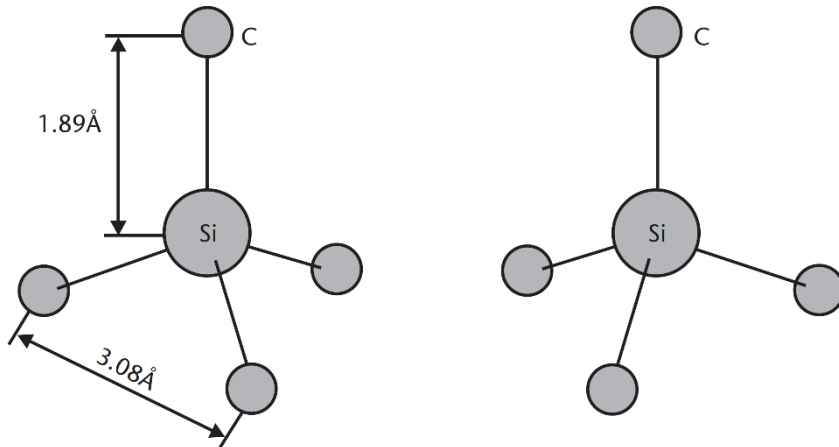


Figure 1.7. The characteristic tetrahedron building block of all SiC crystals. Four carbon atoms are covalently bonded with a silicon atom in the center. Two types exist. One is rotated  $180^\circ$  around the c-axis with respect to the other, as shown. [6]

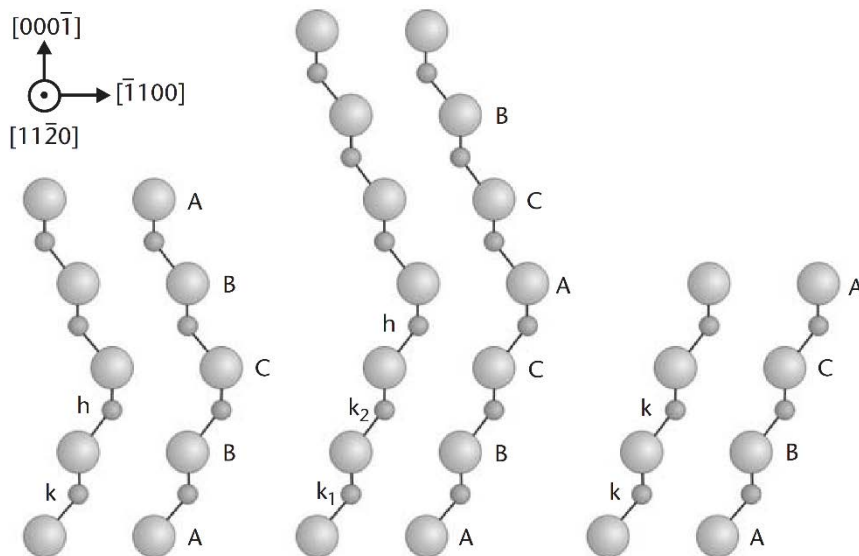


Figure 1.8. The three most common polytypes in SiC viewed in the  $[11\bar{2}0]$  plane. From left to right, 4H-SiC, 6H-SiC, and 3C-SiC; k and h denote crystal symmetry points that are cubic and hexagonal, respectively. [6]



### **1.2.2 Thermal properties**

SiC is suitable for use in a high temperature environment than Si. Thermal properties of Si, 3C-SiC, 4H-SiC and 6H-SiC are shown in Table 1.1. [7, 9-12] The thermal conductivity of SiC is about two to three times higher than that of silicon, and 6H-SiC is the largest among the polytypes of SiC. The decomposition temperature of SiC is also very high, about 2839°C. Power semiconductors are often used in high temperature environments, so they must have good thermal conductivity and must withstand high temperatures. The thermal properties of SiC are suitable for power device.

Table 1.1. Thermal conductivity, thermal expansion coefficient, and decomposition temperature of SiC polytypes.

	Si	4H-SiC	6H-SiC	3C-SiC
<b>Thermal conductivity</b> (Wcm <sup>-1</sup> K <sup>-1</sup> )	1.5 [9]	3.7 [10]	4.9 [10]	3.2 [10]
<b>Thermal expansion coefficient</b> (K <sup>-1</sup> )	$2.7 \times 10^{-6}$ [11]	-	$4.1 \times 10^{-6}$ for a-axis [12] $3.9 \times 10^{-6}$ for c-axis [12]	$2.9 \times 10^{-6}$ [12]
<b>Decomposition (melting) temperature</b> (°C)	1414	-	-	$2839 \pm 40$ [7]

### 1.2.3 Optical properties

The optical properties of the material are related to the band diagram. SiC is a transparent material with a large band gap, and the color changes slightly depending on the doping concentration. SiC also has an indirect band gap in all polytypes. Generally, as the hexagonality increases, the bandgap increases. [13] Table 1.2 shows the hexagonality, the optical band gap at room temperature, and the energy gap at 0K of various SiC polytypes. [13, 14] The band gap of Si is 1.12 eV. 4H-SiC has a band gap about three times larger than that of Si, which lowers on-resistance and reduces power consumption at high temperatures and high frequencies.

Table 1.2. Hexagonality, optical band gaps, and exciton energy gap of various SiC polytypes. [13, 14]

	3C-SiC	6H-SiC	15R-SiC	4H-SiC	2H-SiC
Hexagonality [13]	0	33	40	50	100
Optical bandgap (eV, R.T.) [13]	2.20	2.86	-	3.26	-
energy gap (eV, 0 K) [14]	2.39	3.02	2.99	3.27	3.33

### 1.2.4 Electrical properties

The electrical characteristics are determined according to the material properties of the material, and the role of the semiconductor device is the most important consideration. The electrical properties of SiC polytypes, Si, GaAs, and GaN are listed in Table 1.3. [13] Although SiC does not have the basic electron mobility or hole mobility compared to GaAs, which has the advantage of Si or logic devices, SiC has a strong point in the breakdown electric field and saturated electron drift velocity which are more important in the power device environment such as high voltage and high frequency.

Although the simple material properties can be determined for the suitability of the material to be fitted to the power device, there are various equations, called figure of merit, to determine the suitability on power device. Johnson's figure of merit (JFM), Keyes' figure of merit (KFM), Baliga's figure of merit (BFOM), and combined and dimensionless figure of merit (CFOM) are listed in Table 1.4 for various semiconductors. [15-18]

The JFM is the value of the suitability of materials in high frequency and high voltage applications. The JFM is as following Eq. 1.1; [15]

$$\text{JFM} = \frac{E_B^2 v_S^2}{4\pi^2} \quad \text{Eq. 1.1}$$

where  $E_B$  is the breakdown electric field and  $v_S$  is the saturated electron drift velocity. SiC has a much higher JFM than other materials, which means it is a very suitable material for high voltage and high frequency. Next, the KFM is based on the switching speed of transistor, which is as following Eq. 1.2; [16]

$$\text{KFM} = \kappa \sqrt{\frac{c v_S}{4\pi \epsilon_r}} \quad \text{Eq. 1.2}$$

where  $c$  is the velocity of light,  $\epsilon_r$  is the relative dielectric constant, and  $\kappa$  is the thermal conductivity. The BFOM, which describes material properties of high power switching, is as following Eq. 1.3; [17]

$$\text{BFOM} = \epsilon_r \mu E_B^3 \quad \text{Eq. 1.3}$$

where  $\mu$  is the electron mobility. In this figure of merit, SiC does not show better values than GaAs or GaN. Finally, M. S. Shur suggests the figure of merits called CFOM, which is combined other figure of merits. The CFOM is as following Eq. 1.4; [18]

$$\text{CFOM} = \frac{\kappa \epsilon_r \mu v_S E_B^2}{(\kappa \epsilon_r \mu v_S E_B^2)_{\text{Si}}} \quad \text{Eq. 1.4}$$

By comparing these figure of merits, we can understand the superiority of SiC as a power semiconductor. Among the polytypes of SiC, 4H-SiC has excellent electrical properties and many researches have been made. In this dissertation, 4H-SiC was also used to fabricate and evaluate the device.

Table 1.3. The electrical properties of 3C-SiC, 4H-SiC, 6H-SiC, Si, GaAs, and GaN

	3C-SiC	4H-SiC	6H-SiC	Si	GaAs	GaN
Electron mobility ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )	1000	900	450	1500	8500	900
Hole mobility ( $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ )	50	100	50	450	400	20
Breakdwn electric field ( $\times 10^6 \text{ Vcm}^{-1}$ )	2	3	3	0.3	0.4	3
Saturated electron drift velocity ( $\times 10^7 \text{ cm}^{-1}$ )	2.7	2.2	1.9	1	2	2
Relative dielectric constant	9.7	10.0	10.0	11.9	12.8	10.4

Table 1.4. The figure of merits for various semiconductors. [15-18]

	JFM	KFM	BFOM	CFOM
Si	1.0	1.0	1.0	1.0
GaAs	6.9	0.456	15.7	7.36
InP	16.0	0.608	-	-
GaN	281.6	1.76	24.6	404
6H-SiC	695.4	5.12	-	393
4H-SiC	932.3	5.51	-	404
3C-SiC	1137.8	5.81	4.4	-
Diamond	8206.0	32.2	101	30080



## 1.3 Gate Oxide Issue for SiC MOS Device

### 1.3.1 Conventional SiC MOSFET

As shown in Chap. 1.1.2, the Si MOSFETs are excellent semiconductor devices. In the fabrication of the MOSFETs, Si has the advantage of forming a very stable oxide film through thermal oxidation. Fortunately, SiC also formed stable SiO<sub>2</sub> by thermal oxidation although higher temperatures are required than Si. Therefore, SiC MOSFETs can take the form of Si and can make a lateral MOSFET such as Fig. 1.4, which is a basic MOSFET type. However, the first power MOSFET structure commercially introduced by the power semiconductor industry was the double-diffused or D-MOSFET structure. [19] B. J. Baliga reported in [19] as following;

“The channel length of this device could be reduced to sub-micron dimensions by controlling the diffusion depths of the P-base and N+ source regions without resorting to expensive lithography tools.”

The D-MOSFET structure is shown in Fig. 1.9. [19] When a voltage is applied to the gate, the channel is opened. Unlike the lateral MOSFET, a p-n junction (JFET region) is formed at the center of the gate and current flows to the substrate. Theoretically, the minimum on-resistance of a D-MOSFET is given by Eq. 1.5; [20]

$$R_{ON} = \frac{V_B^2}{\mu_N \epsilon_S E_C^3} \quad \text{Eq. 1.5}$$

where  $R_{ON}$  is the on-resistance,  $V_B$  is the voltage blocked by the MOSFET,  $\mu_N$

is the bulk electron mobility perpendicular to the semiconductor/oxide interface,  $\epsilon_s$  is the permittivity of SiC and  $E_c$  is the critical field. However, the on-resistance of real D-MOSFET device is a larger value than theoretical value due to the parasitic resistance at each point where the current flows. The real on-resistivity is following Eq. 1.6 as shown Fig. 1.10; [19]

$$R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD} \quad \text{Eq. 1.6}$$

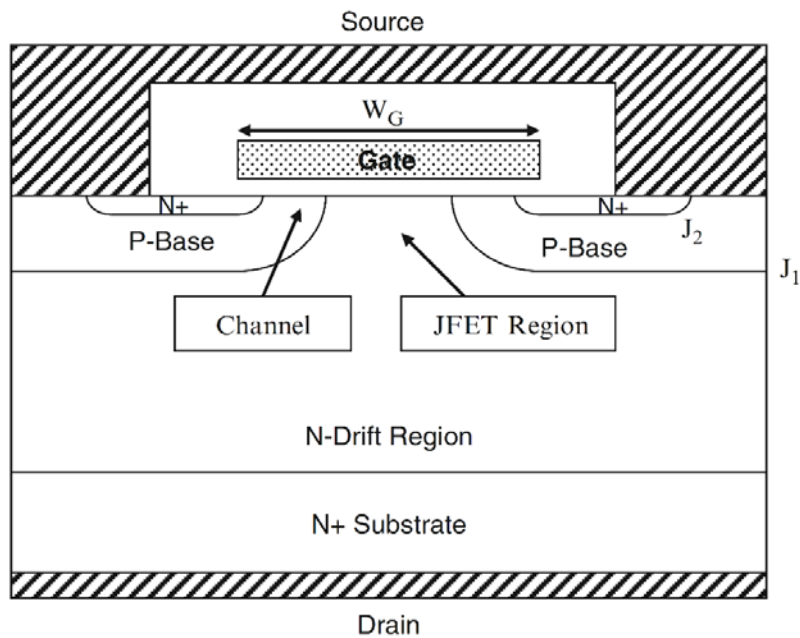


Figure 1.9. The D-MOSFET structure. [19]

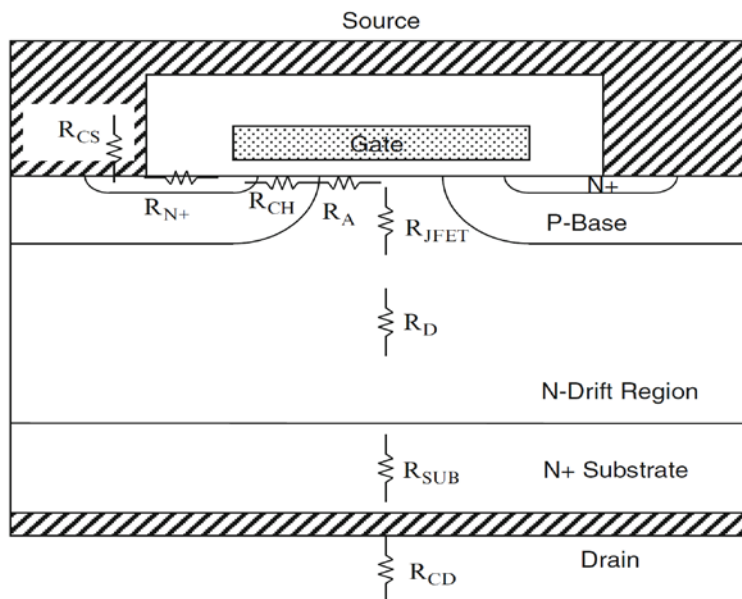


Figure 1.10. Power D-MOSFET structure with its internal resistances. [19]

### 1.3.2 The formation of defect between SiO<sub>2</sub>/SiC interface

As you can see in Chap. 1.3.1, real semiconductor devices are hard to have the theoretical electron and hole mobility due to parasitic resistance. On the other hand, a defect is also generated between the oxide film and the SiC substrate, which is called interface state or interface trap. The interface state means an energy state that should not exist in an ideal device in the oxide film and semiconductor interface. [21, 22] Electrons and holes can be trapped in the interface state, which causes the mobility of carriers to be lowered, which causes deterioration of device performance. The interface state exists due to the dangling bond in the Si device, but the interface state can be reduced by the forming gas annealing (FGA), where H atoms are replacing the dangling bond.

When SiC is oxidized to form SiO<sub>2</sub>, another type of interface state is formed. Interface state density ( $D_{it}$ ) levels of various SiC polytypes and Si and the cause of interface state are shown in Fig. 1.11. [23] Except for dangling bonds, carbon clusters are a factor that increases the  $D_{it}$  level by one order. The carbon clusters are known to be formed by excess carbon remaining in the oxidation process. [24-27] In order to form SiO<sub>2</sub>, Si-C bonds must be cut off and Si-O bonds should be formed. In this case, the remaining C atoms form C-O or C-C bond. C-O molecules can diffuse out from SiO<sub>2</sub>/SiC interface, but C-C clusters remain interface. These clusters form the interface state.

P. Deák et al. analyzed the mechanism of defect creation at the SiC/SiO<sub>2</sub> interface by calculation (Fig. 1.12). [24] According to their report, “the hole traps near the valence band edge originate from carbon-carbon bonds, while carbon dangling bonds are responsible for the amphoteric states deep in the

band gap. ... Silicon interstitials give rise to a broad distribution of electron traps a little farther from the CB (conduction band) edge, while the sharp peak of electron traps with critically high density at about 0.1 eV below the CB edge of 4H-SiC are most likely due to carbon dimers substituting two nearby oxygen atoms in the silica network.” Although these reports covered new defects, carbon clusters have the largest portion in the end, and many papers have shown that the interface state produced by the carbon cluster is the deterioration of electron mobility.

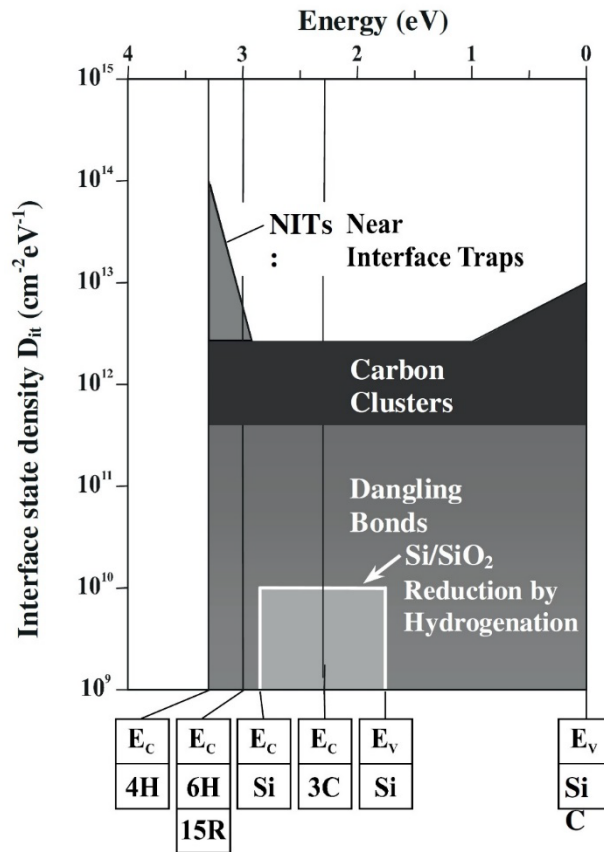


Figure 1.11. Comparison of interface state density at the SiO<sub>2</sub>/SiC interface of different SiC polytypes and at the SiO<sub>2</sub>/Si interface reduced by hydrogenation. [23]

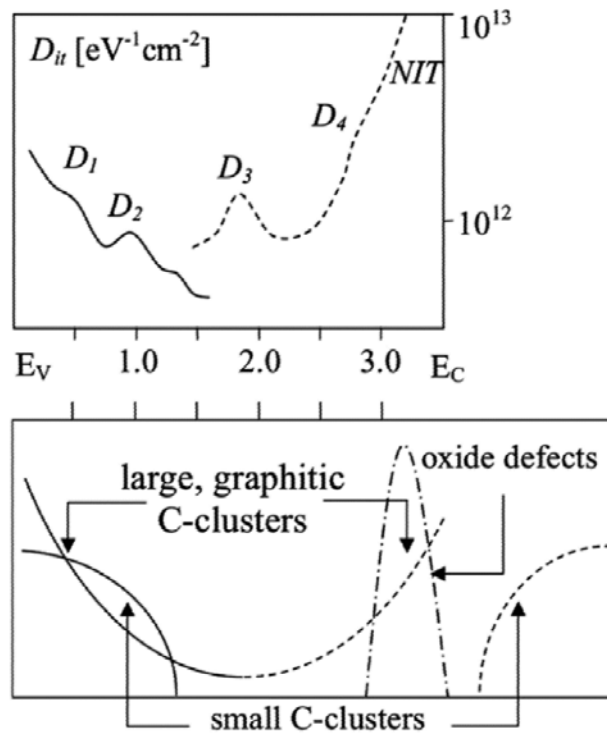


Figure 1.12. Schematic overview of the experimental data on the  $D_{it}(E)$  at the 4H-SiC/SiO<sub>2</sub> interface (top) and the carbon cluster model for explanation of the  $D_{it}(E)$  (bottom). [24]

## Chapter 2. Literature Review

### 2.1 Fabrication Method of Gate Oxide

#### 2.1.1 Thermal oxide on SiC

Thermal oxide means the gate oxide fabricated by thermal oxidation. As mentioned Chap. 1.1.3, SiC can form SiO<sub>2</sub> by oxidation. This is the reason why SiC is ahead of other competing power semiconductors because SiO<sub>2</sub> serves as a very stable insulating film. The thermal oxidation divided to two methods. The first is dry oxidation using only O<sub>2</sub> gas as oxidant, and the second is wet oxidation using H<sub>2</sub>O gas or H<sub>2</sub>/O<sub>2</sub> mixed gas. The oxidation process of SiC can be summarized by the following reactions; [28]



That is, there are five steps in the oxidation process of SiC: [29] 1) transport of molecular O<sub>2</sub> gas to the oxide surface; 2) in-diffusion of the O<sub>2</sub> through the oxide film; 3) reaction with SiC at the oxide/SiC interface; 4) out-diffusion of product gases through the oxide film; 5) removal of product gases away from the oxide surface. Among these five steps, step 1) and 5) are fast steps, and the remaining three steps are rate determinant steps. [30, 31]

The oxidation of SiC is about one order of magnitude slower than that of Si under the same conditions. [29] In addition, the oxidation rate of SiC varies



depending on the crystal orientation. The oxidation rates of 4H-SiC for various crystal orientation are shown in Fig. 2.1. [32] The results of Fig. 2.1 show that the oxidation rate at the C-face is 1 order faster than the Si-face at the same temperature, and the a-face and m-face have intermediate oxidation rates between those of Si-face and C-face. The reason for the difference in the oxidation rate by crystal orientation depends on the number of Si- bonds to break. When Si atoms on a surface of a SiC substrate are oxidized, it is necessary to break one Si-C back-bond for the C face, two Si-C back-bonds for the a face, and three Si-C back-bonds for the Si face, as shown in Fig. 2.2. [33] The difference in the oxidation rate depending on the crystal orientation does not affect the oxidation of the general plane, but a problem may arise when a gate having a complex structure such as a trench gate, a U-shaped gate, or a V-shaped gate is used. [1]

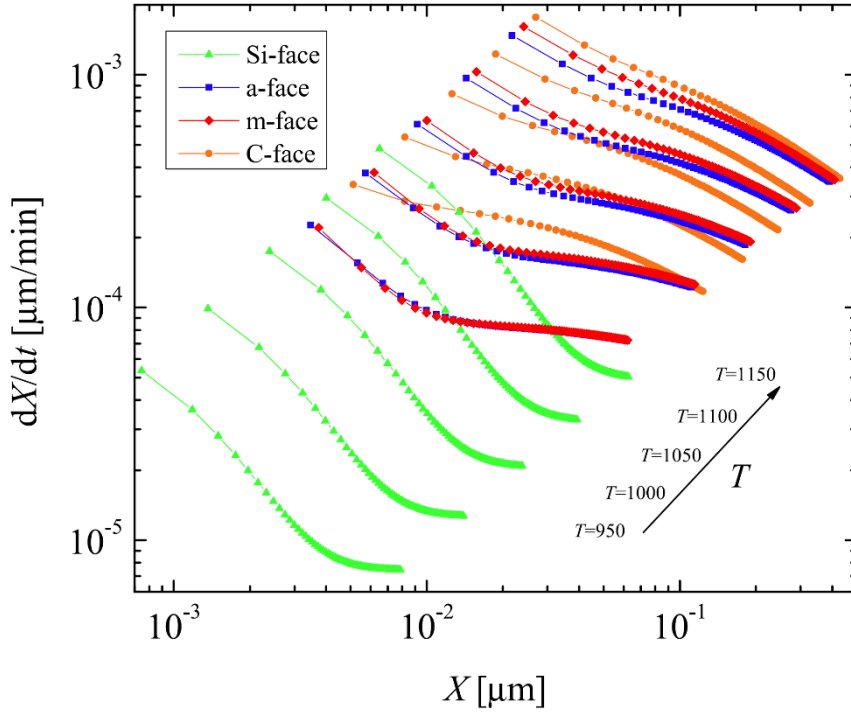


Figure 2.1. Oxide growth rates as a function of oxide thicknesses at various temperatures for the (0001) Si- (green triangles), the  $(11\bar{2}0)$  a- (blue squares), the  $(1\bar{1}00)$  m- (red diamonds), and the  $(000\bar{1})$  C-face (orange circles) of 4H-SiC dry thermal oxidation. [32]

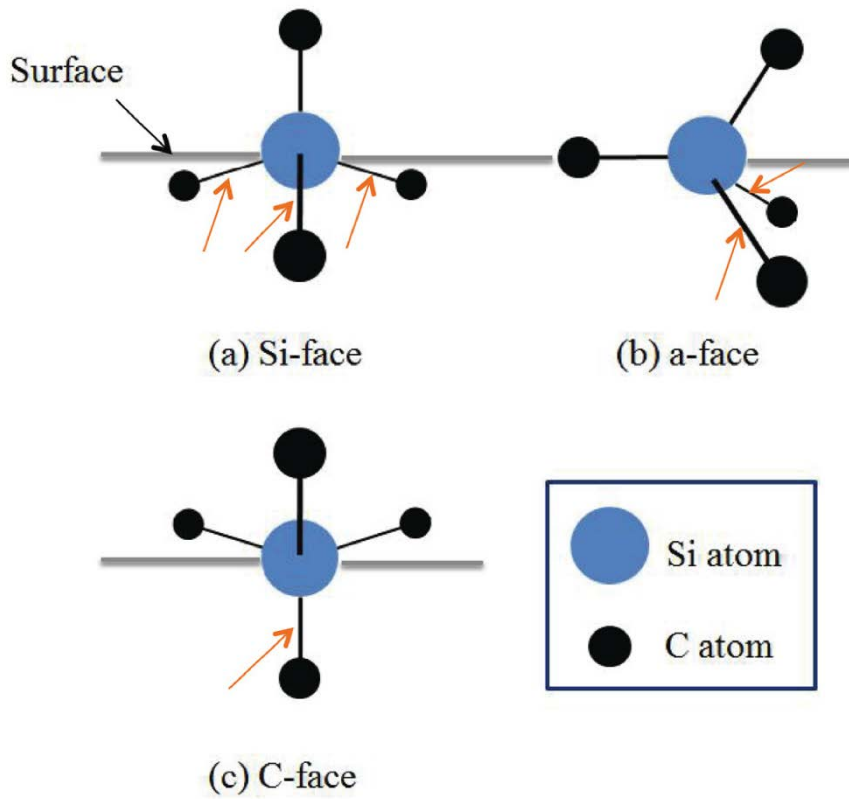


Figure 2.2. Schematic diagrams of Si-C bonds on the SiC surface. The orange arrow denotes Si back-bond. [33]

### 2.1.2 CVD oxide

Chemical vapor deposition (CVD) is a typical method for depositing insulating films of semiconductor processes. Fig. 2.3 shows the step-by-step process of CVD. [34] The CVD has an advantage in that it can be deposited regardless of the surface state of the thin film such as materials, structure or roughness. In addition, various compounds and insulating films can be deposited from ball bearing and cutting tools to rocket engines and nuclear reactors. The CVD in semiconductor fabrication has been used for epitaxial layer growth, gate insulating films, device isolation, planarization, and passivation. [35]

Generally, the CVD  $\text{SiO}_2$  deposition is performed by the reaction of  $\text{SiH}_4$  and  $\text{O}_2$ . In order to facilitate the low-temperature deposition, an organic precursor such as TEOS (tetraethyl-orthosilicate) is used, which is called metal-organic CVD (MOCVD), and plasma enhanced CVD (PECVD), which is a method of using plasma to enhance reactivity, is also used. Furthermore, High Density Plasma (HDP) CVD technology is being developed for superior gap-fill characteristics. In addition, for highly conformal step coverage, the CVD may be performed at temperatures higher than  $700^\circ\text{C}$ .

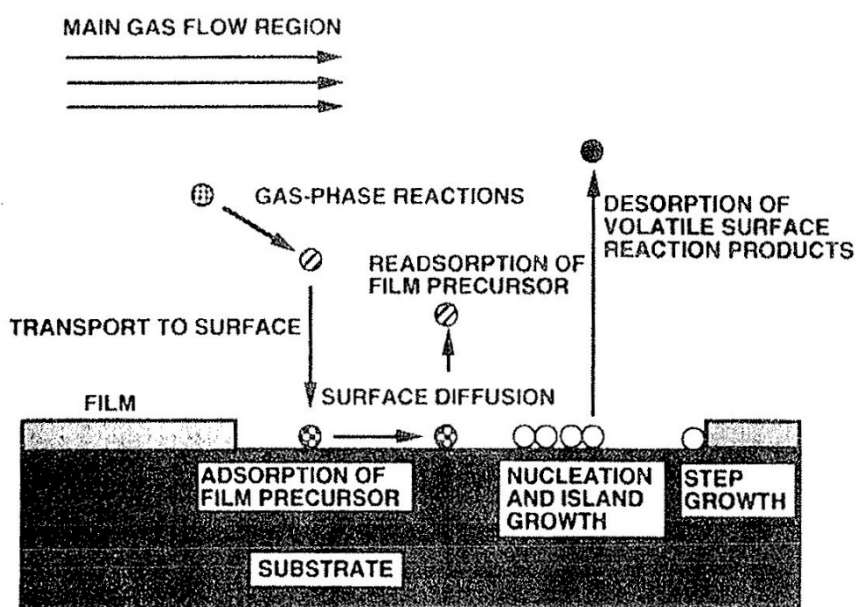


Figure 2.3. Reaction principle and steps of CVD. [34]

### 2.1.3 ALD oxide

Atomic Layer Deposition (ALD) is a method of depositing metal thin films and insulating films in modern semiconductor processes. Fig. 2.4 shows the four step of ALD behavior. [36] In the first step, a precursor carried Ar gas is flowed into a deposition chamber to be adsorbed on the substrate. In the second stage, only the Ar gas is flowed into the chamber. At this time, the remaining precursor excluding the single layer adsorbed on the substrate surface diffuses out of the deposition chamber. In step 3, the oxidant like  $O_2$ ,  $O_3$ , and  $H_2O$  is flowed to the deposition chamber. The oxidant then reacts with the precursor, and formed one monolayer of oxide film. In step 4, the byproducts such as chlorine, hydrogen, or carbon of the precursor are pumped out by blowing the Ar gas again. These step 1 to 4 are defined as one cycle, and one cycle made one monolayer of films. The ALD method has the advantage of precisely controlling thin thickness from Å to nm.

Recently, a metal-organic ALD (MOALD) method is mainly used. In MOALD, metal-organic precursors, which has carbon bonds like ethyl and methyl, are used for deposition. Furthermore, a plasma enhanced ALD (PEALD) is used, and various ALD studies have been carried out. In particular, it is used for the formation of high-k dielectric such as  $HfO_2$  in the logic device and the memory to replace  $SiO_2$ .

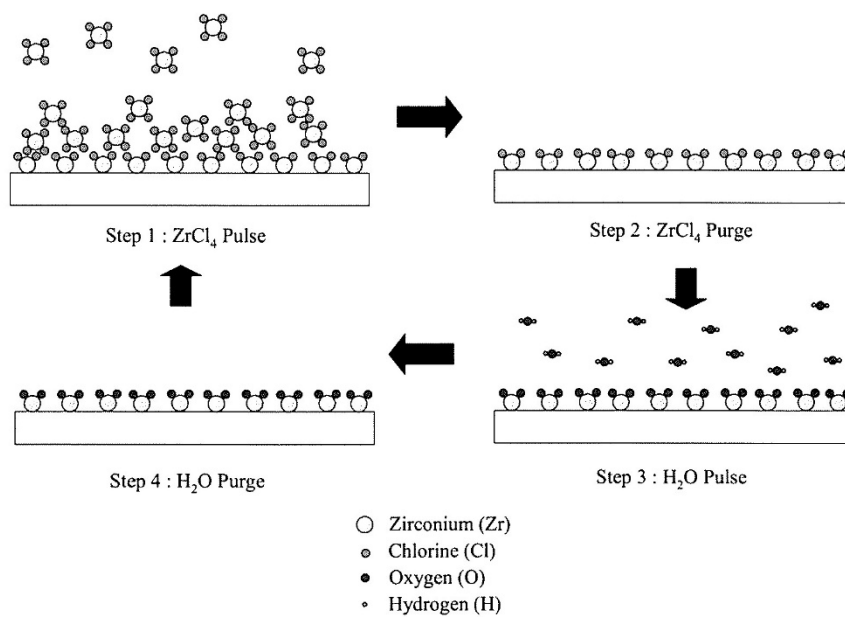


Figure 2.4. 4 step of ALD: 1) source pulse, 2) source purge, 3) reactant pulse, 4) reactant purge. [36]

### 2.1.4 PVD oxide

Physical vapor deposition (PVD) is a physical adsorption method rather than a chemical reaction. PVD has two types of evaporation and sputtering. Evaporation is a method of vaporizing a raw material by evaporation, which is mainly used for metal deposition. Since the oxide has a high melting point, evaporation is impossible. However, sputtering is the method of sputtering and taking away the target by using Ar ion, so that the deposition of the oxide is possible. The schematics of DC and RF sputtering systems are shown in Fig. 2.5.

Sputtering is advantageous in that it can be deposited at a lower temperature than CVD and does not require the use of toxic gas such as  $\text{SiH}_4$ . Sputtered oxide can be used to micro-electro-mechanical systems (MEMS) application like cantilever beams, micro-bridge, membrane etc. [37] However, due to the limitation of the physical vapor deposition, it is pointed out that the formation of oxygen-deficient thin film are the limitations. In addition, to obtain an accurate control of the composition and thickness is not an easy task, and this restriction has a severe impact on the selective sensitivity of the film. [38]



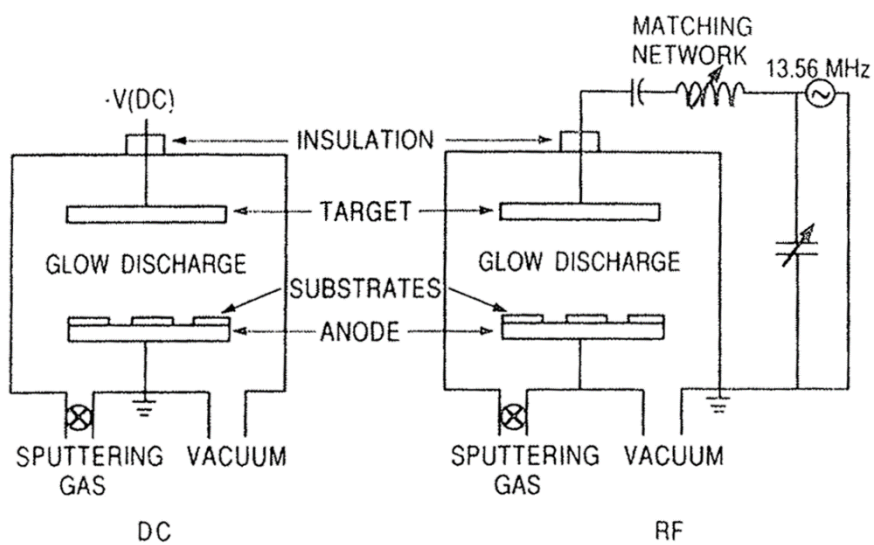


Figure 2.5. Schematics of simplified sputtering system: (a) DC, (b) RF.

## 2.2 Nitridation of SiO<sub>2</sub> on SiC for MOS device

In Chap. 2.1, the basic principles of deposition have been discussed. SiO<sub>2</sub> is used for the SiC MOS device by such oxidation/deposition method, and the study of the characteristics of the device for each oxide film forming method is actively progressing. Before reviewing the electrical properties of each oxide, post-oxidation annealing (POA) and post-deposition annealing (PDA) must be discussed. Basically, NO gas POA is used to remove carbon clusters generated in the oxidation process, and many POA and PDA studies have been conducted based on NO POA.

The reactions and mechanism of reducing C defects by NO POA are illustrated in Fig. 2.6. [39] NO POA plays two roles, the first is the removal of carbon and the second is passivation through Si–N bonds formation. Even if N<sub>2</sub>O gas is used, the similar effect as NO gas can be obtained. N<sub>2</sub>O gas decomposes at high temperatures to form NO and O<sub>2</sub> molecules. However, when using N<sub>2</sub>O gas, the O<sub>2</sub> partial pressure is higher than when NO gas is used, so that re-oxidation due to O<sub>2</sub> will occur more than when NO gas is used.

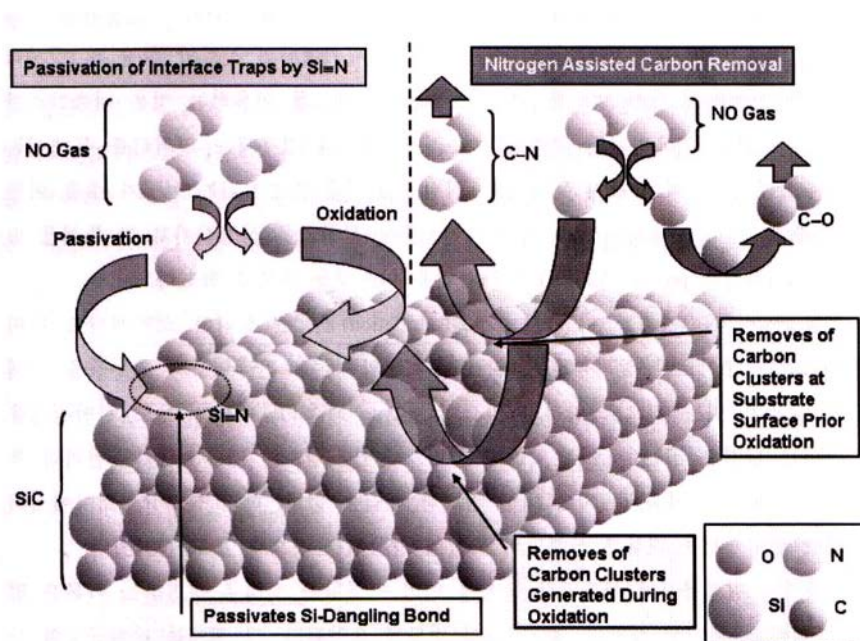


Figure 2.6. The schematic diagram of nitridation. [39]

### 2.2.1 NO and N<sub>2</sub>O post-oxidation annealing

In 1997, H. Li et al. reported the interfacial characteristics of NO nitrided SiO<sub>2</sub> grown on n-type 6H-SiC. [40] They grew the SiO<sub>2</sub> by RTP at 1100°C, and two sets of samples were further exposed to NO or N<sub>2</sub>O annealing, respectively, for an additional 5 min at around 1100°C. Fig. 2.7 shows D<sub>it</sub> level of their MOS capacitors. The D<sub>it</sub> of RTP-grown SiO<sub>2</sub> is smaller than thermal oxidized SiO<sub>2</sub>. In addition, after NO POA, the D<sub>it</sub> is even smaller than RTP-grown SiO<sub>2</sub>. This report is almost the first report to improve the interfacial properties using NO. [41]

P. Jamet and S. Dimitrijević reported N<sub>2</sub>O and NO-nitrided gate oxides grown on 4H-SiC in 2001. [42] In this report, NO and N<sub>2</sub>O POA proceeded for 1.5 h after 3 h of dry oxidation, 6 h oxidation using NO and N<sub>2</sub>O also conducted. The *capacitance–voltage* (*C–V*) characteristics of MOS capacitor with NO, N<sub>2</sub>O, and Ar annealed oxide and NO and N<sub>2</sub>O grown oxide in the paper are shown Fig. 2.8. Generally, there are many D<sub>it</sub> when the *C–V* curve is laid. From this point of view, it can be considered that NO POA oxide and NO grown oxide have the best interfacial properties. In x-ray photoelectron spectroscopy (XPS) analysis, authors stated like the following comments; “It reveals existence of suboxides and complex oxide–carbon compounds at the interface of Ar-annealed oxide... In the case of nitrided oxides, however, the XPS results reveal a significantly different interface: The complex suboxide and oxide–carbon bonds are removed, strong Si–N bonds are created, and the spectral intensity of C–C bonds is significantly reduced. These results can explain the established improvements of electrical properties of the NO annealed oxides.” The

secondary ion mass spectroscopy (SIMS) profile also demonstrates that NO and N<sub>2</sub>O nitrided the oxide film in Fig. 2.9.

G. Y. Chung et al. investigate the role of N atoms in passivating C atoms and C clusters by comparison of n-MOS and p-MOS capacitors and density-functional calculations. [43] They compared n-MOS and p-MOS capacitors, and reported that  $D_{it}$  of n-MOS capacitor decreased after NO POA but  $D_{it}$  of p-MOS capacitor increased after NO POA. Fig. 2.10 shows suggested energy levels for interstitial C and C clusters in SiC before and after N passivation. Before N passivation, the C defect level is located near the conduction band edge. At this time, the defect levels are detected by the  $D_{it}$  extraction of the n-MOS capacitor since it becomes a passage of electrons which is a major carrier of the n-MOS capacitor. After the NO POA, the energy band is located near the valence band edge. This is detected in the  $D_{it}$  extraction of the capacitor of the p-MOS capacitor. That is, after N passivation, the energy levels of C defects shift from the conduction band edge to the valence band edge.

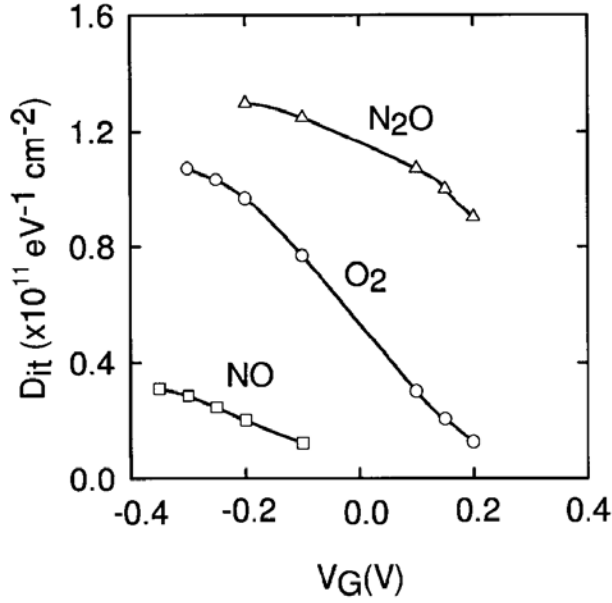


Figure 2.7. Interface state density versus gate voltage for MOS capacitors with three different types of dielectrics. [40]

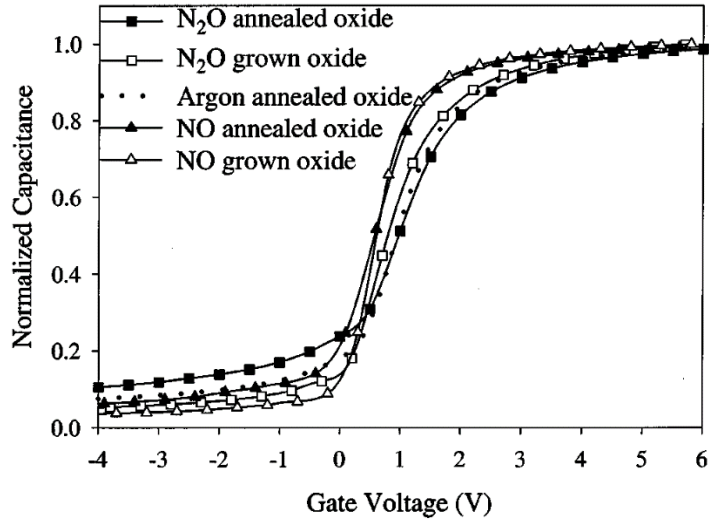


Figure 2.8. Typical normalized HF C-V curves of both NO and N<sub>2</sub>O annealed/grown oxides and Ar annealed oxides. [42]

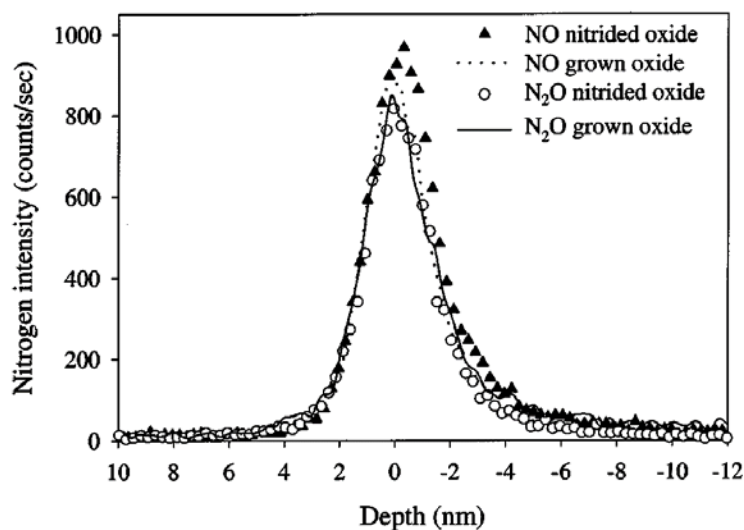


Figure 2.9. Nitrogen SIMS profiles through NO nitrided (black triangle), NO grown (dotted line),  $\text{N}_2\text{O}$  nitrided (white circle), and  $\text{N}_2\text{O}$  grown (line) oxides grown on 4H SiC. [42] (The depth scale was established from the sputtering rate, calculated from the sputtering time corresponding to 50% of oxygen intensity—labeled as “0 nm”; the oxide thickness was measured from the accumulation capacitance of corresponding MOS capacitor.)

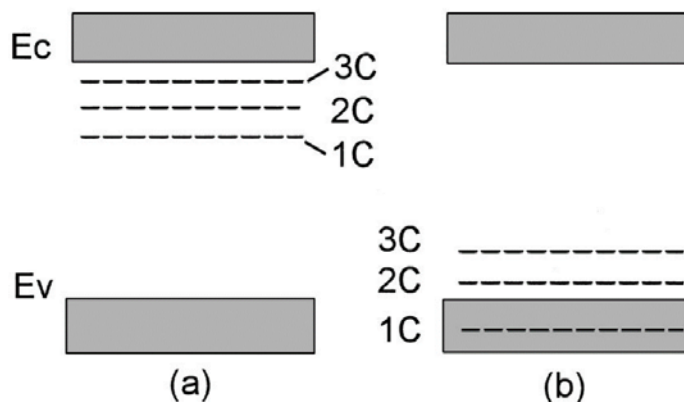


Figure 2.10. (a) Energy levels for interstitial C and C clusters in SiC. (b) C and C cluster states in SiC following N passivation. [43]

### 2.2.2 N<sub>2</sub> post-oxidation annealing

NO and N<sub>2</sub>O POA are accompanied re-oxidation by O atoms as well as nitridation by N atoms. To reduce this re-oxidation effect, POA should be done with pure nitrogen. However, nitrogen is chemically stable compared to NO and N<sub>2</sub>O, requiring higher temperatures for nitridation. In Fig. 2.11, N 1s XPS spectra of the N<sub>2</sub> POA samples with various annealing temperature after completely removing the SiO<sub>2</sub> layers are shown. [44] In this results, it is probably difficult for stable nitrogen molecules to react at the interfaces under the inadequate annealing temperatures below 1350°C. On the other hand, the N 1s peak intensities taken from the samples with N<sub>2</sub> POA at 1400°C increased considerably. That is, N<sub>2</sub> POA requires a high temperature above 1400°C to ensure the nitridation effects.



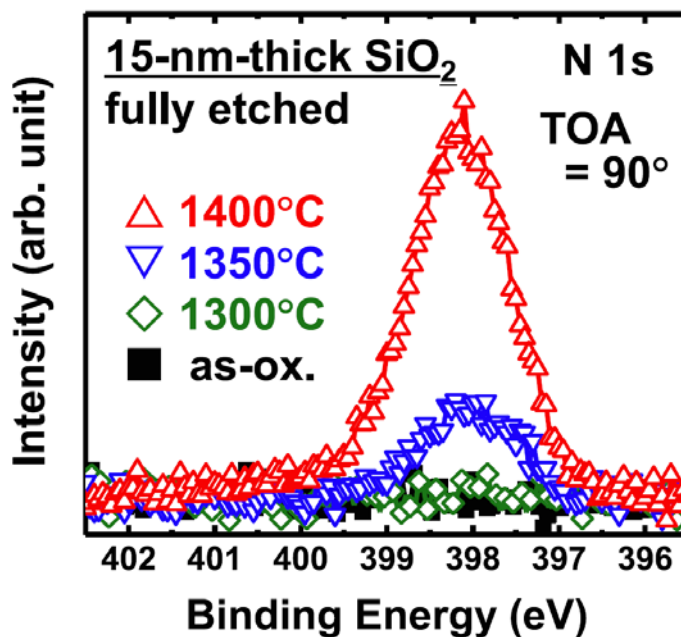


Figure 2.11. Change in the N 1s core-level spectra obtained from the N<sub>2</sub>-POA treated SiC samples with 15-nm-thick thermal SiO<sub>2</sub> layers after complete SiO<sub>2</sub> removal. The POA in pure N<sub>2</sub> ambient was done for 30 min at different temperatures, i.e. 1400°C (upward red triangles), 1350°C (downward blue triangles), and 1300°C (green rhombuses). The as-oxidized SiO<sub>2</sub>/SiC sample without post annealing (black filled squares: as-ox.) is also shown for comparison. Peak intensity was normalized by the Si 2p peak intensities (not shown). [44]

### 2.2.3 Other nitridation methods

Not only the conventional furnace POA methods were investigated, but also studies on the other nitridation methods have been carried out.  $N_2$  plasma treatment is one of them. [45, 46] The  $D_{it}$  results of plasma treated oxide and standard NO POA to comparison are shown in Fig. 2.12. [45] The  $N_2$  plasma treatment was carried out at  $1160^\circ\text{C}$  for 2, 4, 6 h. Plasma treatments for 2 h had a higher  $D_{it}$  than NO POA, but plasma treatments for 4 h and 6 h were lower than NO POA. This result shows that the nitridation of C cluster is effectively conducted by the plasma. In order to confirm the  $N_2$  plasma effect more directly, XPS results are shown in Fig. 2.13. The XPS results show that the magnitude of N 1s peak is larger in order of 2 h, standard NO, 4 h, 6 h, which is the trend of decreasing  $D_{it}$ . That is, the more nitridation is done, the lower the  $D_{it}$ .

Nitridation using  $HNO_3$  vapor was also proposed. [47] In this experiment, the  $HNO_3$  vapor was oxidized with  $H_2O$  on the 4H-SiC substrate. A bubbler containing  $HNO_3$  solution was heated at various temperatures; 60, 70, 80, 90, 100, and  $110^\circ\text{C}$ . As the amount of  $HNO_3$  increased, the  $D_{it}$  decreased, which is similar to other nitridation processes. In addition,  $HNO_3/H_2O$  oxidized  $SiO_2$ . SIMS analysis showed that nitrogen bonding was not present in the  $SiO_2$  bulk but only in the  $SiO_2/SiC$  interface, which could be interpreted that the nitridation process had little effect on the chemical bonding of  $SiO_2$  bulk. The SIMS results of C,  $CN^-$ ,  $Si^-$ , and  $SiN^-$  were shown in Fig. 2.14. As the  $HNO_3$  vaporizing temperature increases, the C intensity decreases, which seems to reduce the C cluster. At this time,  $CN^-$  tends to decrease above  $90^\circ\text{C}$ , which is believed to be due to the formation of CO and  $CO_2$ .  $SiN^-$  intensity also increased

as  $\text{HNO}_3$  vaporizing temperature increasing. This is also because it forms Si–N passivation. These results show that the removal of C cluster and the Si–N passivation, which are the principle of improving properties in NO POA, are applied similarly in  $\text{HNO}_3$ .

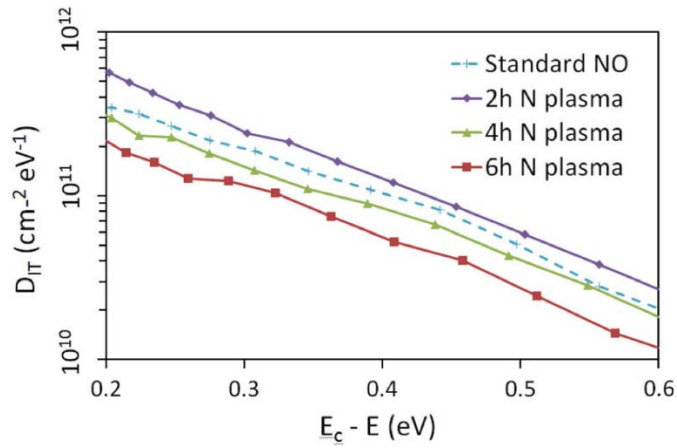


Figure 2.12. Relationship between  $D_{it}$  measured for each process and energy from conduction band between 0.2 eV and 0.6 eV. The  $D_{it}$  measured at 0.2 eV steadily decreases as the nitrogen plasma POA time increases. [45]

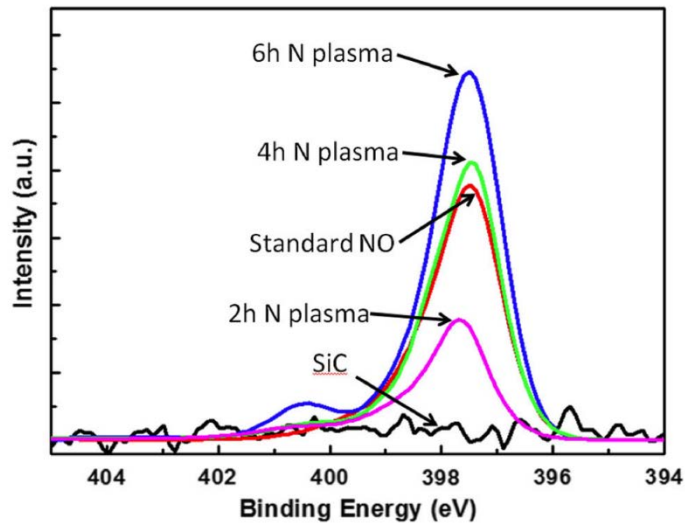


Figure 2.13. XPS profile of the N 1s nitrogen at the  $\text{SiO}_2/\text{SiC}$  interface after oxide etch. [45]

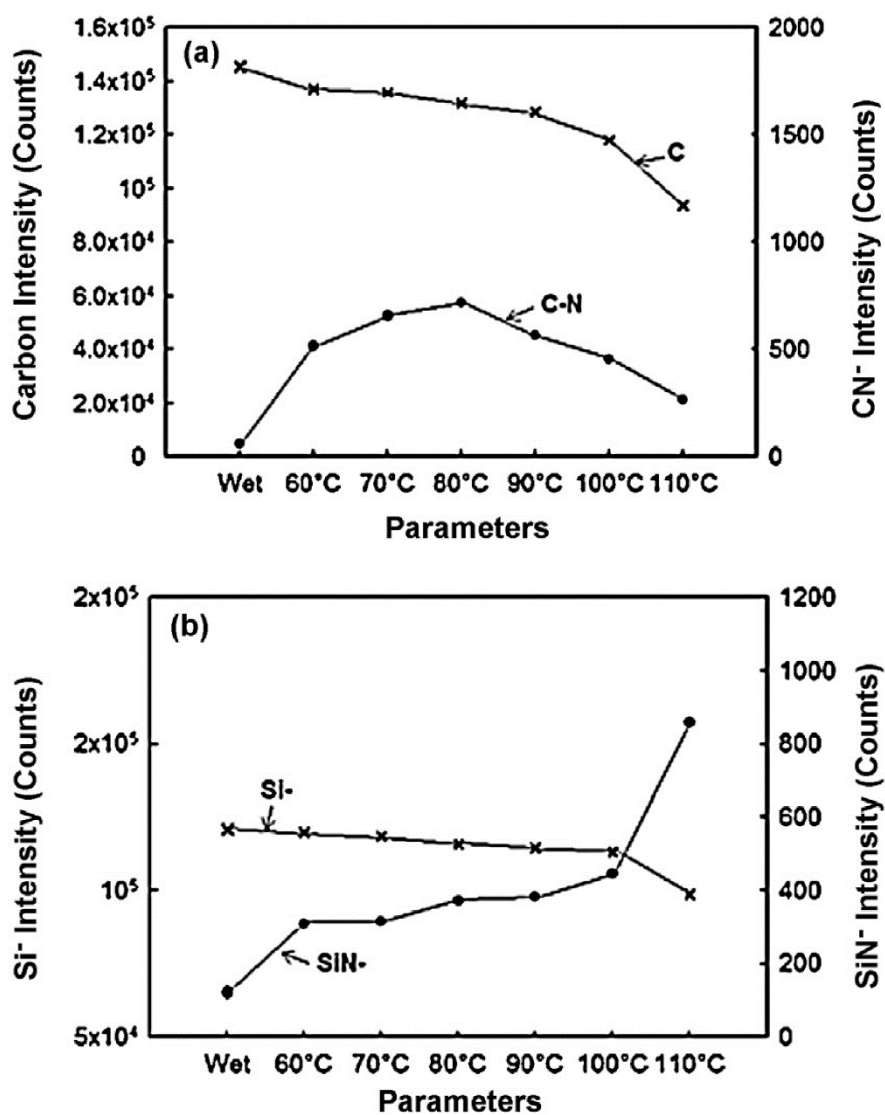


Figure 2.14. Correlation graphs of extracted peak of species intensity values from SIMS characterization for all samples. (a) Carbon intensity and CN<sup>-</sup> intensity, (b) Si<sup>-</sup> intensity and SiN<sup>-</sup> intensity. [47]

## 2.3 Basic of Device Measurement

This chapter will cover the measurement of capacitors. Inevitably, in the preceding chapters, electrical characteristics such as  $C-V$  or  $D_{it}$  are presented to compare the characteristics of POA. Including this characteristics, more textual content will be discussed in this chapter. Since many researches on semiconductor measurements have mainly been conducted in Si devices, it will be covered in this chapter. After that, the difference between Si and SiC devices are discussed.

### 2.3.1 $C-V$ measurement

MOS capacitors, also called metal-insulator-semiconductor (MIS) capacitors, are devices that can be easily manufactured and measured for electrical properties. MOS capacitor is divided into three states according to the gate voltage. The three states of p-MOS capacitor on Si are shown in Fig. 2.15: [48] accumulation, depletion, and inversion, and  $C-V$  characteristics are shown in Fig. 2.16. [49, 50] At accumulation, majority-carriers (holes in case of p-MOS capacitor) are accumulated from semiconductor to  $\text{SiO}_2/\text{Si}$  interface. As gate voltage increasing, accumulated majority-carrier are moved to the opposite side of the oxide, and MOS capacitor enters the depletion region at  $0 < \psi_s < \phi_F$ . When the voltage becomes higher, it becomes inversion and minority carriers are attracted to the  $\text{SiO}_2/\text{Si}$  interface. As shown in Fig. 2.16, in accumulation, the majority carriers react regardless of the low frequency and the high

frequency, but in inversion, the minority carriers react only to the low frequency.  
[49, 51]

The electrical characteristics of the real device differ from the ideal  $C-V$  due to impurities, unintended charges, and defects. The defect charges in real MOS device are classified into 4 types with respect to their location and action, which are interface state charges ( $Q_{it}$ ), fixed charge ( $Q_f$ ), dielectric-trapped charges ( $Q_{ot}$ ), and mobile ionic charges ( $Q_m$ ). These defects change the  $C-V$  graph of the device, each with slightly different parts. For example, the fixed charges shifts the position of the  $C-V$  curve as shown in Fig. 2.17, and the interface serves to stretchout the  $C-V$  curve as shown in Fig. 2.18. Therefore, by comparing the ideal  $C-V$  curve with the real  $C-V$  curve, it is possible to judge which charge is affected by the real MOS capacitor by the shift of the flat band voltage and the slope of the  $C-V$  curve.

Without distinguishing each charge, the total amount of oxide charge can be calculated by comparing how the real curve is shifted compared to the ideal curve. This oxide charge is called the effective oxide charge ( $Q_{eff}$ ) density, which is as following Eq. 2.4; [52]

$$Q_{eff} = \frac{\Delta V_{FB} C_{ox}}{q A_G} \quad \text{Eq. 2.4}$$

where  $\Delta V_{FB}$ ,  $C_{ox}$ ,  $q$ , and  $A_G$  are shift of flat band voltage between ideal  $C-V$  and real  $C-V$ , maximum oxide capacitance, electron charge, and gate area, respectively.

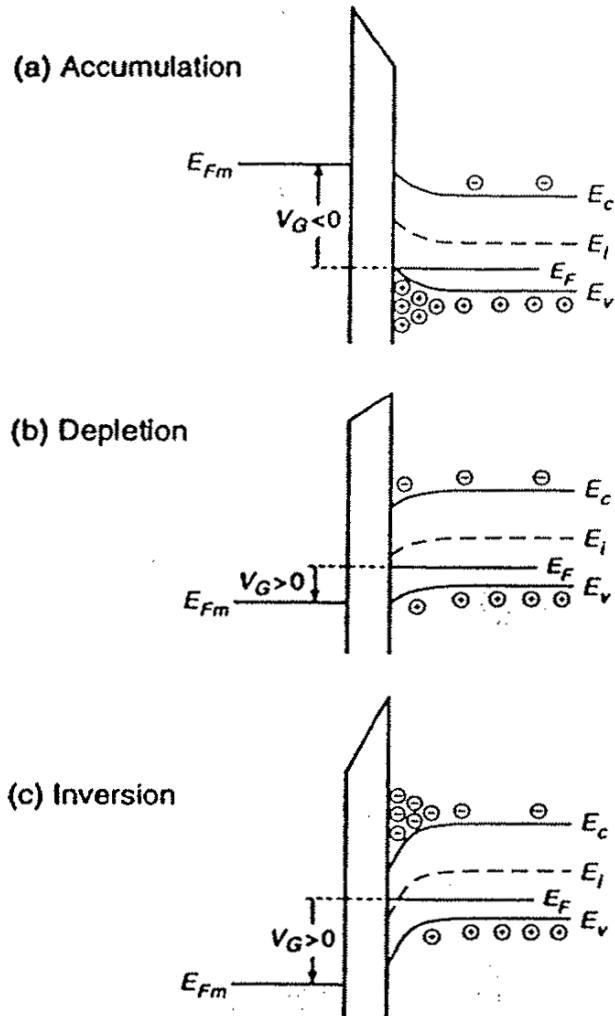


Figure 2.15. Energy-band diagrams of an ideal MOS (MIS) capacitor with a p-type semiconductor at  $V_G = 0$  for (a) accumulation, (b) depletion, and (c) inversion conditions. [48]



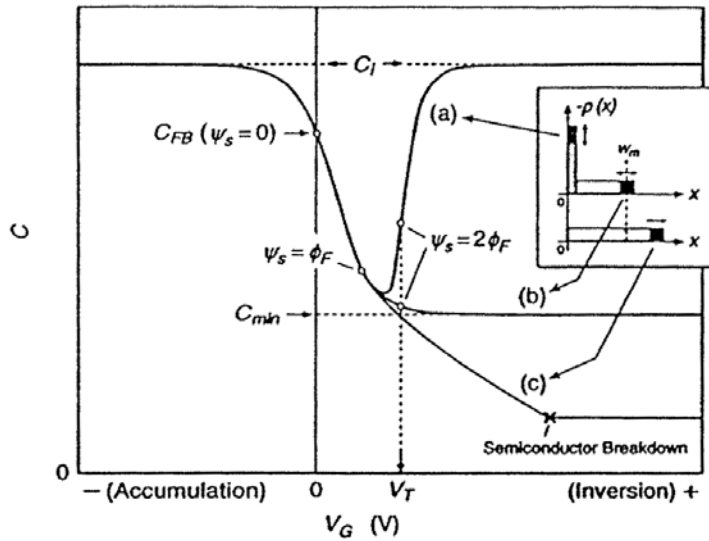


Figure 2.16. MIS capacitance–voltage characteristics under (a) low-frequency, (b) high-frequency, and (c) deep-depletion conditions. [50]

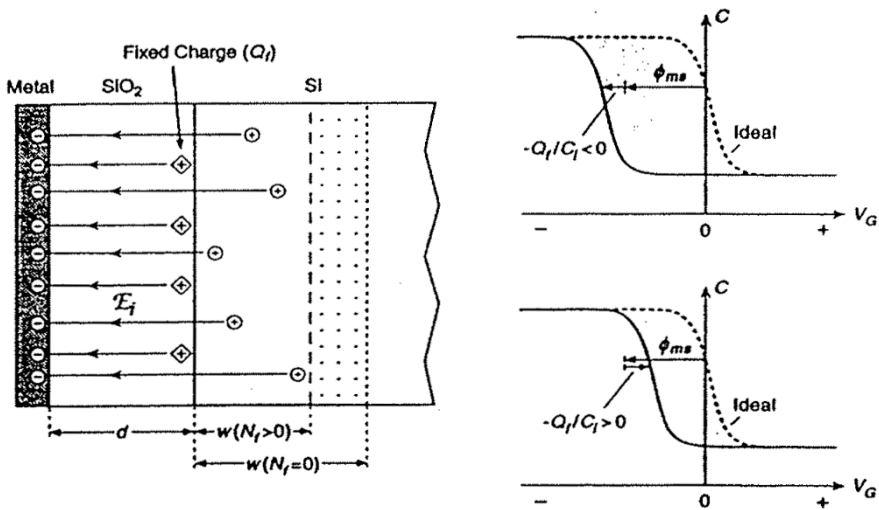


Figure 2.17. Effect of a fixed charge  $Q_f$  on a MIS capacitor with an n-type semiconductor (left), [51] and the resulting parallel shifts of the  $C$ – $V$  curves relative to ideal ones for a p-type semiconductor (right). [49]

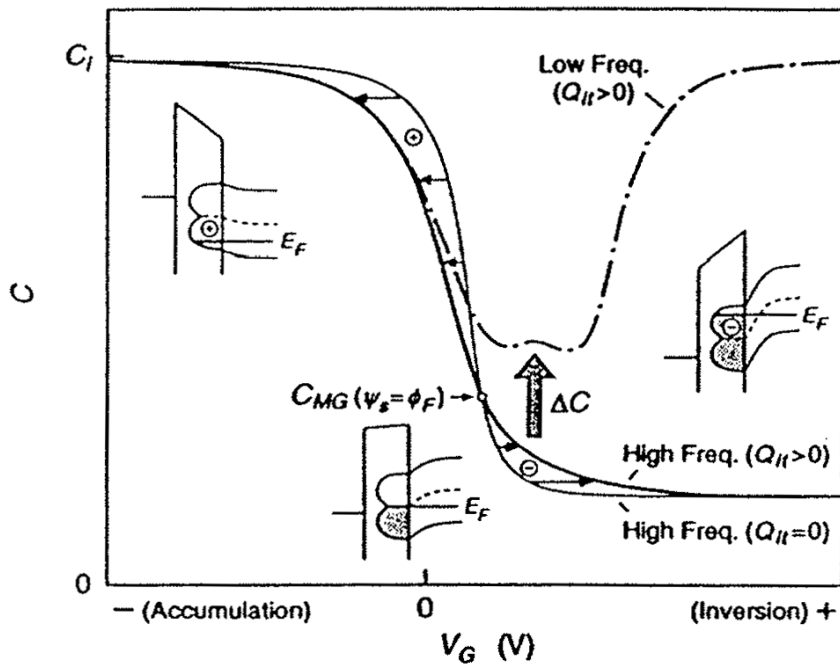


Figure 2.18. Stretchout in  $C$ - $V$  curves due to interface-state charge  $Q_{it}$ . [49]

### 2.3.2 Interface state density measurement

Among the defects, the interface trap is important at the SiC/SiO<sub>2</sub> interface, because C clusters at the SiC/SiO<sub>2</sub> interface exist in the form of interface traps. The interface state density ( $D_{it}$ ) of SiC can be extracted using extraction methods of Si MOS device by changing only the parameters. There are 3 most commonly used methods for  $D_{it}$  extraction of MOS devices: [52] 1) Terman method (or high-frequency method), 2) high-low frequency method (low-frequency method or quasi-static method), and 3) conductance method.

First, Terman method is the first method to determine  $D_{it}$  at room temperature and high-frequency. [53] Terman method uses the stretchout of capacitance according to frequency, which is determined by the following Eq. 2.5; [52]

$$D_{it} = \frac{C_{ox}}{q^2} \left( \frac{dV_G}{d\phi_s} - 1 \right) - \frac{C_s}{q^2} = \frac{C_{ox}}{q^2} \frac{dV_G}{d\phi_s} \quad \text{Eq. 2.5}$$

where  $V_G$ ,  $\phi_s$ ,  $C_s$ , and  $\Delta V_G$  are gate voltage, surface potential, surface capacitance, and shift between ideal  $V_G$  and real  $V_G$ , respectively.

Seconds, high-low frequency method was developed by Berglund, but Berglund's method had taken a long time. [54] Complementing this, Castagné and Vapaille proposed a simple high-low frequency method as following Eq. 2.6; [55]

$$D_{it} = \frac{C_{ox}}{q^2} \left( \frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad \text{Eq. 2.6}$$

where  $C_{lf}$  and  $C_{hf}$  are low-frequency (quasi-static) capacitance and high frequency capacitance.

Finally, conductance method is proposed by Nicollian and Goetzaberger, which is a highly accurate method. [56] This method is based on the processes trapped and released in the interfacial trap, which is a method of measuring the equivalent parallel conductivity,  $G_p$ . The equivalent circuit is shown in Fig. 2.20 to understand the conductivity method. Fig. 2.20(a) and (b) show the basic circuit and simplified circuit. Here, the  $G_p$  is determined as following Eq. 2.7;

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \quad \text{Eq. 2.7}$$

where  $\omega = 2\pi\nu$  ( $\nu$  = measurement frequency) and  $\tau_{it} = R_{it}C_{it}$ . At this time, Eq. 2.7 is for a single energy level captured and emitted by  $D_{it}$ . However, the interface between the semiconductor and the oxide film has a continuous energy level, and thus the normalized conductance of Eq. 2.7 should be obtained, which is as following Eq. 2.8; [56]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad \text{Eq. 2.8}$$

Finally,  $D_{it}$  is extracted at the point of maximum capture/emission, which is the maximum point of  $G_p/\omega$ . The approximate  $D_{it}$  is as following Eq. 2.9; [56]

$$D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{max} \quad \text{Eq. 2.9}$$

Meanwhile, in general, capacitance in  $C-V$  measurement does not distinguish capacitance between oxide and semiconductor, and it is analyzed as in Fig. 2.20(c) when measured by parallel mode. Although it is difficult to obtain  $\tau_{it}$ ,  $G_p$  can be obtained using a measured equivalent circuit as following Eq. 2.10; [51]

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad \text{Eq. 2.10}$$

Using the Eq. 2.9 and Eq. 2.10, the  $D_{it}$  can be extracted using parallel mode capacitance measurement in wide frequency range. The conductance method is equally applicable to SiC by changing the substrate parameters.

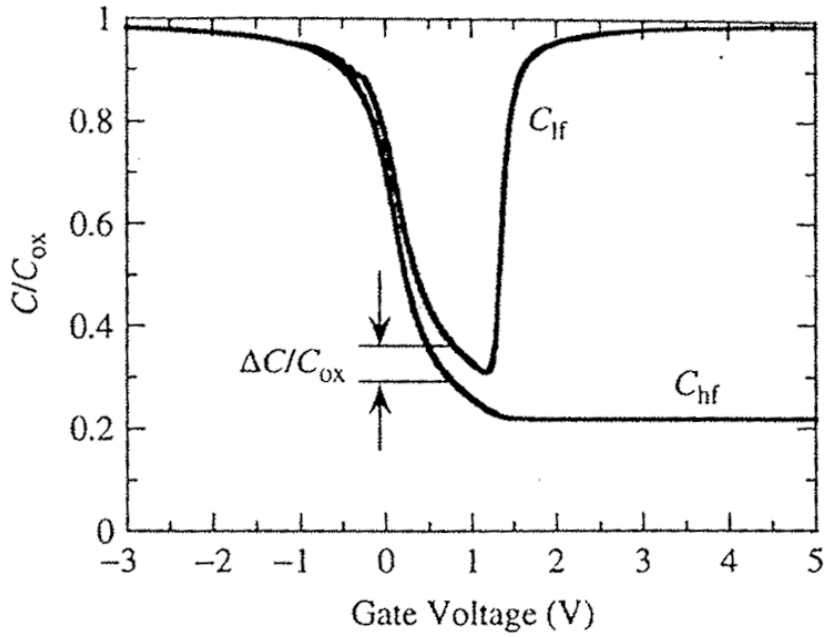


Figure 2.19. High- and low-frequency  $C$ - $V_G$  curves showing the offset  $\Delta C/C_{ox}$  due to interface traps. [52]

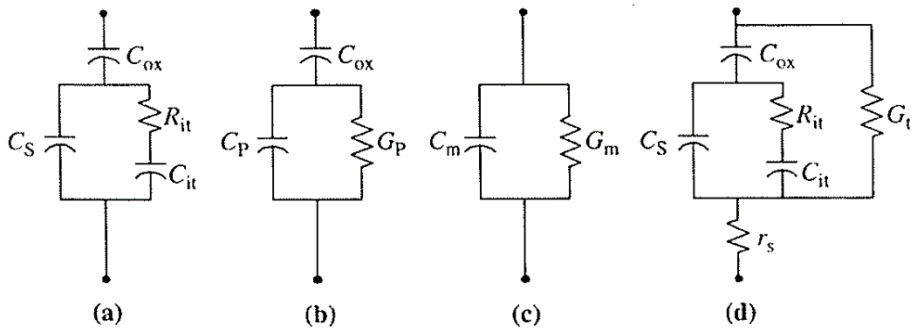


Figure 2.20. Equivalent circuits for conductance measurements; (a) MOS-C with interface trap time constant  $\tau_{it} = R_{it}C_{it}$ , (b) simplified circuit of (a), (c) measured circuit, (d) circuits including series resistance ( $r_s$ ) and tunneling conductivity ( $G_t$ ).

### 2.3.3 $J$ - $E$ measurement

Although there is an insulator between the metal and the semiconductor in the MOS capacitor, the current is not completely cut off. The *current density–oxide electric field* ( $J$ - $E$ ) can be obtained by the leakage current and gate voltage at this time. Fig. 2.21 shows the equations and illustrations of five representative mechanisms through which the current can flow through the insulator. [49] Among them, Schottky emission is mainly observed at low voltage and Fowler-Nordheim (F-N) tunneling is caused at high voltage between SiC and SiO<sub>2</sub>. In general, F-N tunneling occurs at an extremely high voltage in case of Si device, but SiC has a higher bandgap of about 2 eV and a higher conduction band than Si, resulting in F-N tunneling at a voltage of about 6 MV/cm.

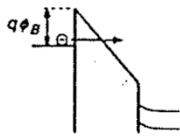
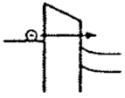
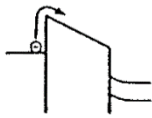
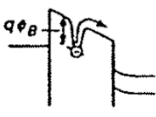

Fowler-Nordheim Tunneling	$J = \frac{A}{4\phi_B} E_i^2 \cdot \exp\left(-\frac{2B\phi_B^{3/2}}{3E_i}\right)$	
Direct Tunneling	$J = \frac{A}{d^2} \left\{ \left(\phi_B - \frac{V}{2}\right) \cdot \exp\left(-Bd\sqrt{\phi_B - \frac{V}{2}}\right) - \left(\phi_B + \frac{V}{2}\right) \cdot \exp\left(-Bd\sqrt{\phi_B + \frac{V}{2}}\right) \right\}$	
Schottky Emission	$J \propto T^2 \cdot \exp\left(-\frac{\phi_B - \sqrt{E_i/C}}{\phi_i}\right)$	
Poole-Frenkel Emission	$J \propto E_i \cdot \exp\left(-\frac{\phi_B - 2\sqrt{E_i/C}}{\phi_i}\right)$	
Hopping (Ohmic) Conduction	$J \propto E_i \cdot \exp\left(-\frac{\Delta E_{dh}}{kT}\right)$	

Figure 2.21. Typical conduction processes in insulators along with their expressions and illustrations (h: Planck's constant,  $m^*$ : Effective mass of an electron). [49]



## 2.4 Electrical Characteristics of Gate Oxide on SiC

### 2.4.1 Thermal oxide

In studying the electrical properties of SiC MOS capacitors and MOSFETs, thermal oxide is a reference for applied fabrications. In most cases, thermal oxide has been reported to have poor  $C$ – $V$  characteristics and high  $D_{it}$  values compared to more advanced processes such as ALD, NO PDA, etc. However, thermal oxide is highly optimized when it comes to its properties as an insulating film. In this chapter, the electrical properties of  $\text{SiO}_2$  gate oxide itself will be discussed.

The most basic  $J$ – $E$  behavior is shown in Fig. 2.22. [57] Generally, it is known that the  $J$ – $E$  behavior of 4H-SiC n-type MOS capacitors is thermal conduction (Schottky emission) at a voltage less than at 5 MV/cm, and F-N tunneling above that. At high voltage, the F-N tunneling characteristic eventually occurs and it is important to understand the leakage current characteristic. The F-N tunneling formalism is following Eq. 2.11; [58]

$$\ln(J/E_{ox}^2) = \frac{q^3 \left( \frac{m}{m_{ox}} \right)}{8\pi h \Phi_B} - \frac{8\pi \sqrt{2m_{ox}} \Phi_B^3}{3qh} \frac{1}{E_{ox}} \quad \text{Eq. 2.11}$$

The available conduction mechanism of Ni/HfO<sub>2</sub>/4H-SiC capacitors are described in Fig. 2.23. [59] SiC has a larger band gap than Si, and the conduction band is located at a higher energy level. Therefore, when the positive voltage is applied to the n-type MOS capacitor and accumulation occurs, electrons in the conduction band of SiC can easily tunnel to the metal.

Because the gate oxide is  $\text{HfO}_2$  deposited with ALD, Fig. 2.23 describes that four conduction occurs. However, in the case of stable thermal  $\text{SiO}_2$ , there is no trap-filled limit or Poole-Frenkel emission, which conducts through the defect. Direct tunneling is rarely possible when oxide is thicker than 5 nm.

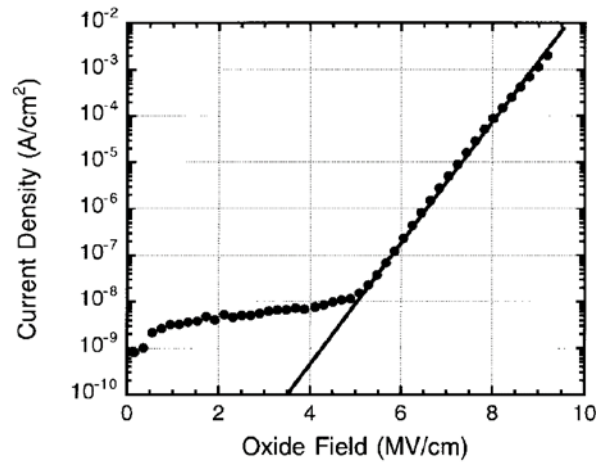


Figure 2.22. Oxide current density as a function of field for an n-type 6H-SiC sample at 140°C. Oxide thickness is 20.5 nm. [57]

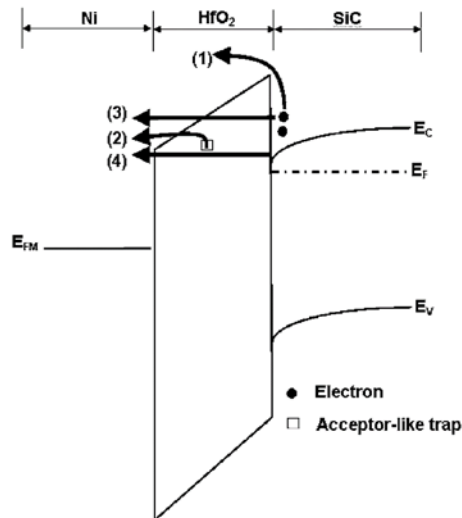


Figure 2.23. Schematic energy-band diagrams of a MOS structure. The numbering (1) – (4) refers to respective leakage paths due to Schottky emission, Poole-Frenkel emission, Fowler-Nordheim tunneling, and direct tunneling.  $E_C$ ,  $E_F$ ,  $E_V$ , and  $E_{FM}$  are the conduction band edge, Fermi level, valence band edge, and Fermi level of Ni, respectively. [59]

### 2.4.2 CVD oxide

Research of the formation of gate oxide by CVD on SiC MOS devices has been investigated since the 1990s. [60-63] Since the research on the deposition of SiO<sub>2</sub> on Si substrate has already been carried out, the CVD oxide on SiC substrate can be deposited and evaluated by using the existing method based on the Si technology. Fig. 2.24 shows the electrical properties of SiO<sub>2</sub> by depositing low-temperature CVD (LTCVD) and subsequent Ar annealing. [60] The as-dep oxide film has a  $V_{FB}$  of 15 V or more because negative oxide charge is included in the oxide film during CVD deposition. As the Ar annealing temperature increased,  $V_{FB}$  approached 0 V, indicating that the Ar PDA was effective for removing interface traps or oxide charge. Since the  $V_{FB}$  of capacitor with non-PDA oxide is moved in the positive voltage, the subsequent PDA must be applied.

The  $D_{it}$  difference between high-temperature CVD (HTCVD) SiO<sub>2</sub> deposited at a high temperature of 950°C and LTCVD SiO<sub>2</sub> deposited at 300°C is shown in Fig. 2.25. [61] In this case, it can be seen that when NO PDA is performed after both HTCVD and LTCVD deposition,  $D_{it}$  has a value similar to that after NO POA after thermal oxidation. These properties demonstrate that the CVD oxide can fully replace the thermal oxide. However, the CVD oxide films showing outstanding characteristics are pointed out as disadvantages in that they operate at relatively high temperatures and use a dangerous gas like SiH<sub>4</sub>.

On the other hand, research on the SiO<sub>2</sub> deposition for SiC MOS gate oxide using MOCVD has also been investigated. A. Pérez-Tomás et al. reported

the measurement of electrical characteristics by depositing gate oxide by MOCVD and PECVD using TEOS and fabricating a capacitor. [62] In this report, amorphous  $\text{SiO}_2$  of 100-nm-thick was deposited at a low temperature of  $430^\circ\text{C}$  by PECVD using TEOS as a precursor on  $8^\circ$  off axis (0001) n-type 4H-SiC substrates. They optimized performance of capacitor by pre-deposition oxidation or PDA.  $D_{it}$  of their MOS capacitor are shown in Fig. 2.26. The only  $\text{N}_2\text{O}$  PDA was not so effective on lowering  $D_{it}$ . Rather  $\text{N}_2$  PDA was more effective than  $\text{N}_2\text{O}$  PDA. However,  $\text{N}_2\text{O}$  pre-oxidation was very effective on lowering  $D_{it}$ . Comparison of the field-effect electron channel mobility ( $\mu_{FE}$ ) in MOSFET with gate oxide made by oxidation and TEOS CVD is Fig. 2.27. The  $\mu_{FE}$  of the oxide film deposited by TEOS after pre-deposition oxidation is superior to that of the standard thermal oxide film. This is considered to be because pre-deposition oxidation plays a role in minimizing plasma damage when PECVD is used.

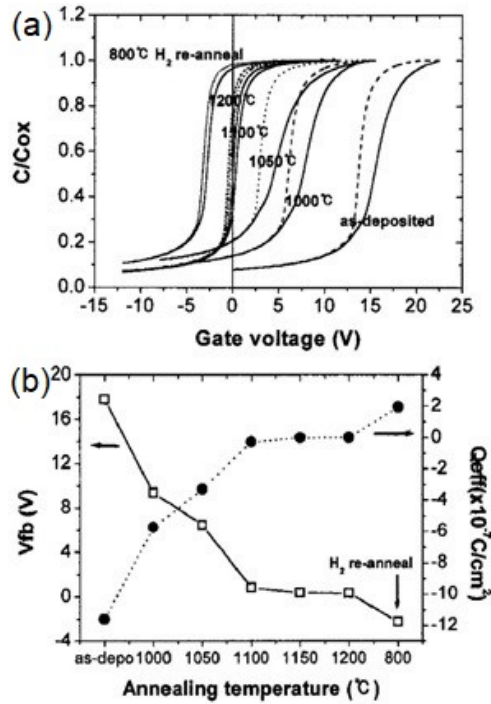


Figure 2.24. (a)  $C$ - $V$  characteristics and (b) extracted  $V_{FB}$  and  $Q_{eff}$  of SiC MOS capacitor with different annealing temperature. Gate oxide of capacitors deposited by LPCVD using SiH<sub>4</sub> and O<sub>2</sub> at 400°C. [60]

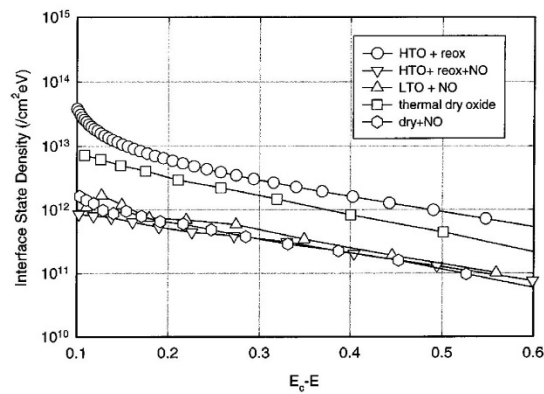


Figure 2.25.  $D_{it}$  of SiC MOS capacitors using CVD oxide and thermal oxide with NO PDA. HTO, LTO, and reox mean HTCVD oxide, LTCVD oxide, and re-oxidation (N<sub>2</sub>, 1h, 950°C), respectively. [61]

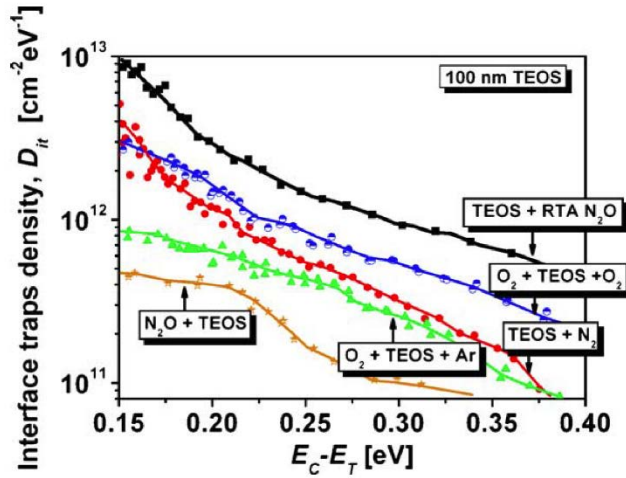


Figure 2.26. Effect of annealing ambients and interfacial oxidation on the interface states density for 4H-SiC MOS capacitors. [62]

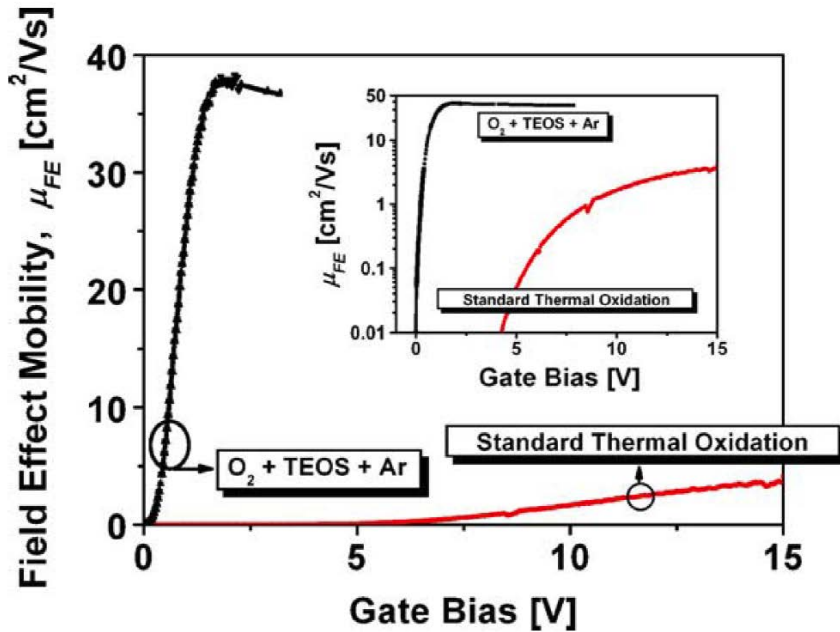


Figure 2.27. Comparison of the field-effect electron channel mobility in transistors with gate made with standard dry oxidation (1150 °C 3 h, O<sub>2</sub>+Ar+950°C Wet Reox), and with 10 nm dry oxide (1050 °C 1 h, O<sub>2</sub>) and SiO<sub>2</sub>-TEOS annealed in Ar. [62]

### 2.4.3 ALD oxide

In order to reduce interface states and to solve the problem of different oxidation rate depending on crystal direction in trench gate, researches continue to deposit oxide films of SiC MOS devices through ALD. Based on the outstanding properties of thickness control and step coverage, recent researches on ALD oxide films are on the rise. [64] As precursors of the SiO<sub>2</sub> deposition, organic precursors like SiH<sub>2</sub>[N(CH<sub>2</sub>CH<sub>3</sub>)<sub>2</sub>]<sub>2</sub> [bis(diethylamino)silane (BDEAS)] and SiH<sub>2</sub>[N(CH<sub>2</sub>)(C<sub>2</sub>H<sub>5</sub>)]<sub>2</sub> [bis(ethylmethylamino)silane (BEMAS)] could be used. In order to deposit using the above precursors, the reactance should have high reactivity, such as O<sub>3</sub> or O<sub>2</sub> plasma. The deposition temperature of the ALD is from room temperature to about 300°C, at a low temperature. In general, the higher the deposition temperature, the better the electrical characteristics of the film.

The *C-V* characteristics of 4H-SiC MOS capacitors with thermally grown oxides and ALD oxides are shown in Fig. 2.28. [65] After oxidation and deposition, NO gas POA or PDA proceeded at 1175°C. In the case of the thermal oxide, as the NO POA time increased from 0 to 120 min, the *C-V* hysteresis decreased and the V<sub>FB</sub> became negative shift. However, when the NO POA time increased to 180 min, the *C-V* hysteresis increased again and the V<sub>FB</sub> returned back to the positive voltage direction. This means that in the case of thermal oxide, the NO POA time of 120 min is the optimal time. When the POA is increased to 180 min, the effects of nitridation by NO gas disappear due to re-oxidation. On the other hand, in the case of the ALD oxide, the *C-V* hysteresis decreased and the V<sub>FB</sub> became negative shift until 180 min of NO



PDA time. It is necessary to examine the difference between the thermal oxidation film and the deposition film. The difference between the thermal oxide film and the deposition oxide film should be noted. It is considered that the ALD oxide film is less chemically stable the oxide film and has a lower density, so the ALD oxide film is considered to be optimized for the NO PDA for a longer period of time than the thermal oxide film.

Fig. 2.29 shows the  $D_{it}$  distributions of thermal oxide with/without NO PDA and ALD oxide with PDA on 4H-SiC. [65] The  $D_{it}$  was measured by high-low  $C-V$  method. The effect of NO POA is obvious in the  $D_{it}$  result of the thermal oxide film with/without NO POA. Moreover, the ALD oxide with NO PDA show extremely low  $D_{it}$  value. Although the reliability of extraction of  $D_{it}$  by high-low  $C-V$  measurement has decreased in recent years, [66, 67] it can be confirmed that the electrical performance of ALD oxide with NO PDA is better than thermal oxide with NO PDA. The electron field effect mobility ( $\mu_{FE}$ ) of the MOSFETs using thermal oxide and ALD oxide is shown in Fig. 2.30 as another evidence for performance improvements. [65] The maximum  $\mu_{FE}$  for thermal oxide without NO PDA, with NO PDA, and ALD oxide with NO PDA were 4.4, 29.7, and 32.4  $\text{cm}^2/\text{V}\cdot\text{s}$ , respectively. In conclusion, when used with optimized PDA, ALD oxide can also exhibit more than thermal oxide properties.

Another paper reported about  $\text{N}_2\text{O}$  PDA effects on ALD oxide. [68] The  $C-V$  characteristics of MOS capacitors with ALD  $\text{SiO}_2$  after  $\text{N}_2\text{O}$  and  $\text{N}_2$  PDA at  $1100^\circ\text{C}$  are shown in Fig. 2.31 at 1 M, 100k, and 10 k-Hz. After  $\text{N}_2$  PDA, the capacitor showed poor  $C-V$  characteristics judging from  $C-V$  slope and frequency dispersion, but the capacitor after  $\text{N}_2\text{O}$  PDA showed good  $C-V$  characteristics.  $\text{N}_2\text{O}$  gas decomposes at high temperatures to form NO, which

can produce similar effects to NO PDA. However, in the case of  $N_2$ , since there is no oxygen, only nitridation effect can be obtained. From this paper,  $N_2O$  has also proven to be effective on ALD films. According to this paper,  $N_2O$  PDA is also effective on electrical properties of ALD oxide films.

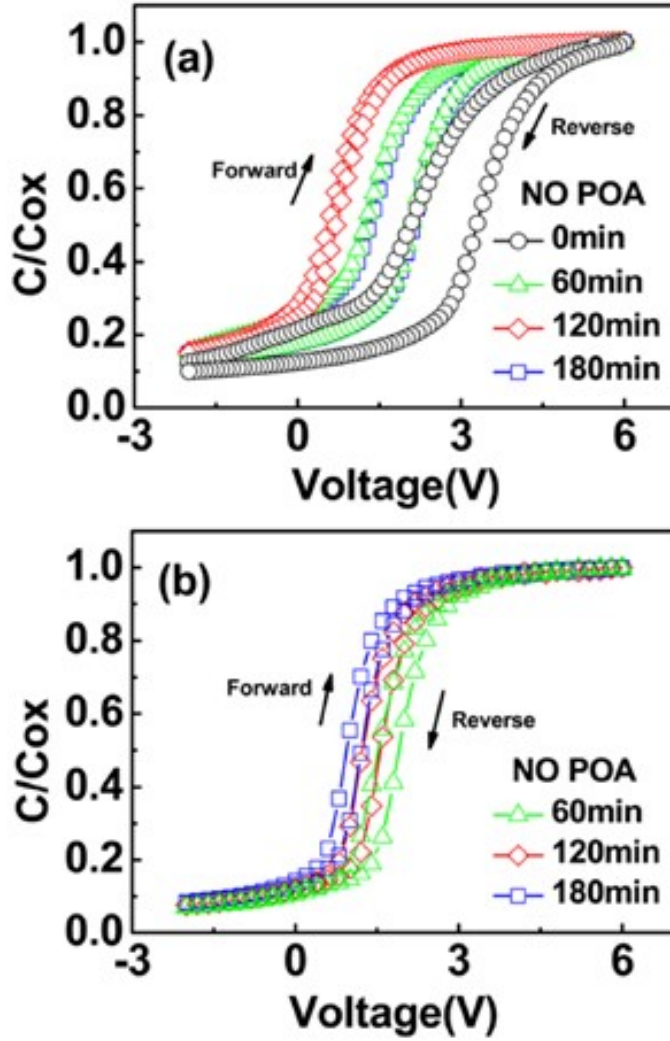


Figure 2.28.  $C$ - $V$  characteristics of MOS capacitors with (a) thermally grown oxides and (b) ALD oxides as a function of NO POA duration. [65]

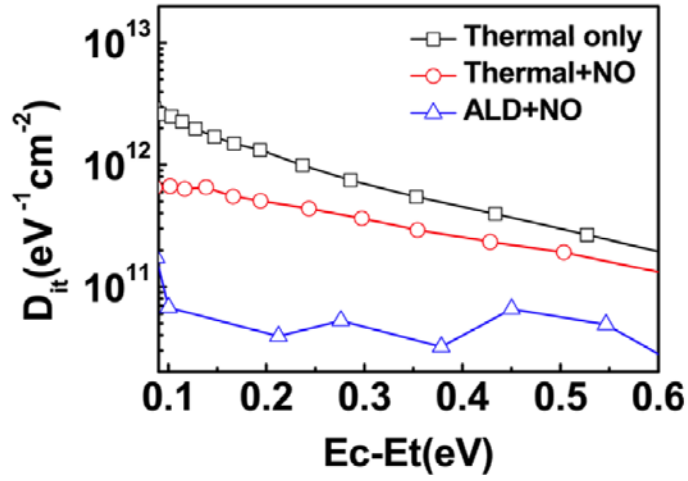


Figure 2.29.  $D_{it}$  distributions as a function of energy level. [65]

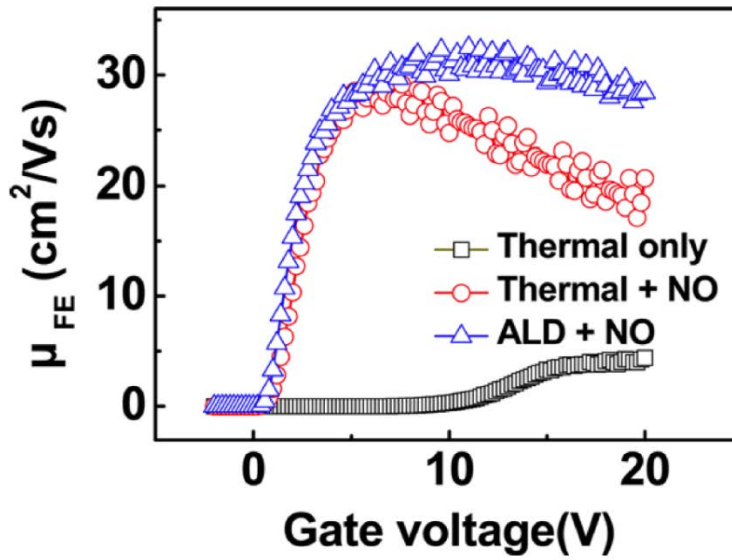


Figure 2.30.  $\mu_{FE}$  of MOSFETs using thermally grown oxide only, thermally grown oxide with 120 min NO POA, and ALD oxide with 180 min NO POA. [65]

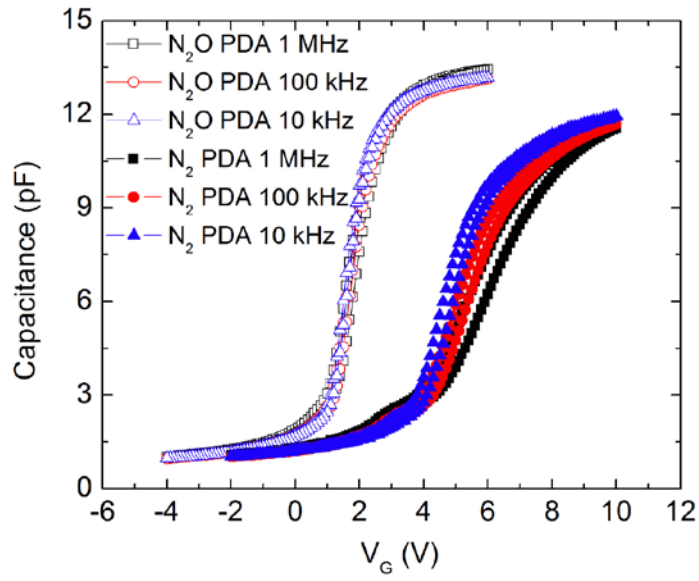


Figure 2.31. 1 M, 100 k, and 10 k-Hz C–V characteristics of MOS capacitors with 30-nm ALD SiO<sub>2</sub> after N<sub>2</sub>O and N<sub>2</sub> PDA at 1100°C. [68]

#### 2.4.4 PVD oxide

Among PVD, oxide or dielectric films such as  $\text{SiO}_2$  are deposited by sputtering. There are few studies on sputtering for SiC MOS, but two of these references have been investigated.

The first paper is the comparison of the surface of the oxide grown by wet oxidation and the oxide grown by sputtering. [69] In this report, sputtering oxide has better surface quality than wet thermal oxide. Fig. 2.32 and Fig. 2.33 shows the atomic force microscope (AFM) image of wet thermal oxide and sputtering oxide, respectively. Before AFM measurement, selective etching was conducted to each sample. In case of wet thermal oxide of Si-face in Fig. 2.32, rough surface appears on oxide surface and etched surface. On the other hand, the both surface of sputtering oxide in Fig. 2.33 is smooth. At the time of wet oxidation, Si atoms on the SiC substrate reacted with the  $\text{O}_2$  molecules on the outside to form  $\text{SiO}_2$ , and the remaining C did not diffuse out, but formed a carbon cluster, resulting in a rough surface. In the case of sputtering, there is no factor to form such a carbon cluster, so the surface state is smooth. In this paper, the growth and surface of sputtering oxide can be compared with thermal oxide, but the optimization of MOS structure is insufficient.

The second paper is about nitridation of 4H-SiC through  $\text{NH}_3$  annealing, and  $\text{SiO}_2$  sputtered on nitride substrate. [70] This paper evaluated the chemical properties of gate oxide and  $I$ - $V$  characteristics of MOS capacitors. In XPS spectra of the Si 2p of nitrified 4H-SiC presented in Fig. 2.34. The Si-N and Si-O-N peaks increased as the  $\text{NH}_3$  annealing temperature increased from 900°C to 1000 and 1100°C. This shows that the nitridation effect of  $\text{NH}_3$

requires increasing the temperature to 1100°C. The  $I$ - $V$  characteristics of MOS capacitors are shown in Fig. 2.35. When gate oxide was deposited on nitrided 4H-SiC, the oxide was not performed as insulator. In general, the PDA improves the oxide film characteristics, but the nitrided 4H-SiC has a poorer property after PDA. This is thought to be due to the diffusion of negative charges, which was generated during  $\text{NH}_3$  annealing in substrate. This paper likewise insufficiently lacks about MOS capacitor optimization.

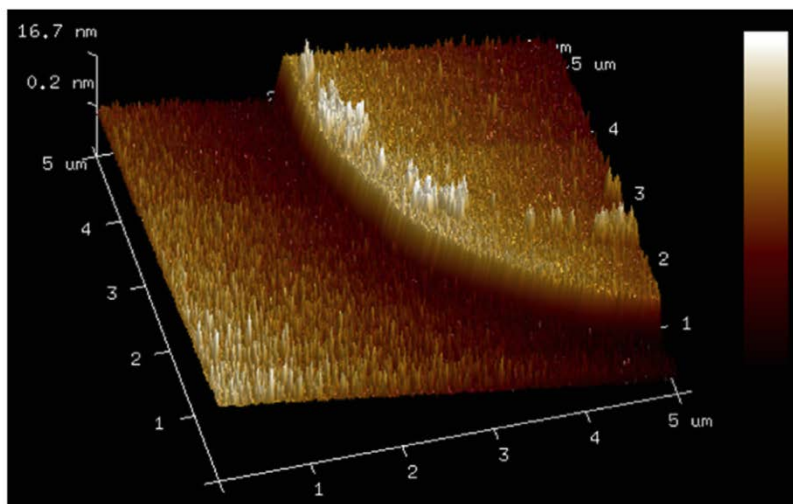


Figure 2.32. Selectively etched SiO<sub>2</sub> layer grown on Si-face SiC substrates by wet thermal oxide process. [69]

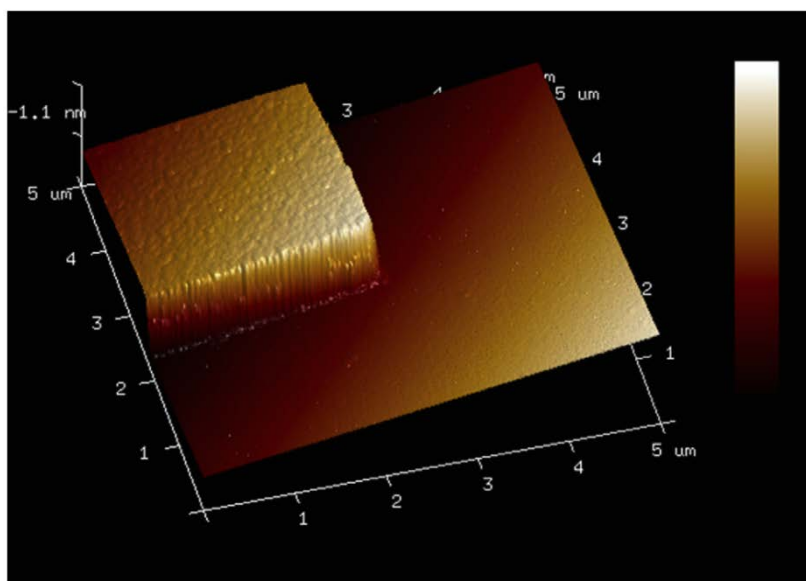


Figure 2.33. Selectively etched SiO<sub>2</sub> layer, which is grown on Si-face 4H-SiC substrate by sputtering. [69]



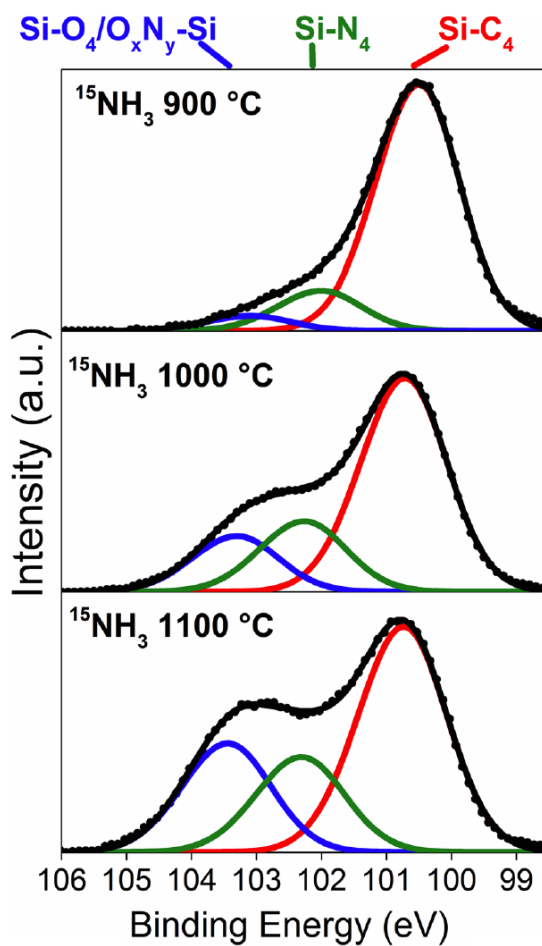


Figure 2.34. Si 2p photoelectron spectra (a.u. stands for arbitrary units) at a take-off angle sensitive to the surface of Si-faced 4H-SiC samples thermally nitrided in 30 mbar of  $^{15}\text{NH}_3$  for 1 h at different temperatures, as indicated. [70]

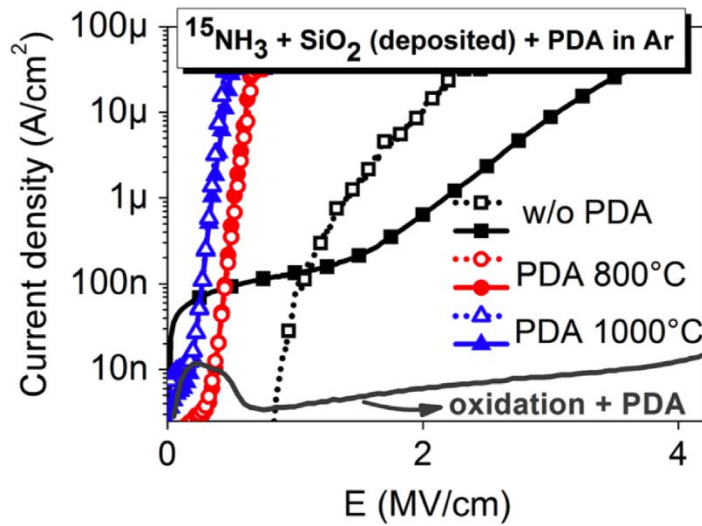


Figure 2.35.  $I$ - $V$  curves of Al/SiO<sub>2</sub>/(nitrided) 4H-SiC structures obtained from 4H-SiC samples submitted to 30 mbar of <sup>15</sup>NH<sub>3</sub> for 1 h at 900°C. (solid symbols) and 1100°C (open symbols) followed by deposition of a 20-nm oxide film by sputtering and addition of Al and GaN contacts. Indicated samples were submitted to PDA in 400 mbar of Ar for 1 h at indicated temperatures. Results from a SiO<sub>2</sub> film formed by SiC thermal oxidation submitted to PDA at 1000°C are also presented for comparison. [70]

## **Chapter 3. Experiment and Analysis**

### **3.1 Sample Preparations**

#### **3.1.1 4H-SiC wafer information**

Commercial 4-inch n-type 4H-SiC epi wafer of production grade made by Cree was used to fabricate MOS capacitors. The orientation of wafer is  $4^\circ$  off-axis and the resistivity is  $0.015\text{--}0.028\ \Omega\cdot\text{cm}$ . The micropipe density (MPD) of the wafer is ultra-low level of less than  $1\ \text{cm}^{-2}$ . Both sides are polished and silicon face is subjected to CMP. Epitaxial layers are deposited on silicon face after CMP. The epitaxial layer consists of two layers: the first layer is  $0.5\ \mu\text{m}$  thick with  $1 \times 10^{18}$  of n-doping concentration and the second layer is  $12\ \mu\text{m}$  thick with  $5 \times 10^{15}$  of n-doping concentration. All capacitors were fabricated on epitaxial layer of silicon face.

#### **3.1.2 Wafer cleaning process**

The wafers were diced to  $8\ \text{mm} \times 8\text{mm}$  and the cleaning process was carried out on samples prior to fabrication of MOS capacitors. The cleaning process was carried out in the following order. First, solvent cleaning was carried out to remove the organic bond used for dicing. For solvent cleaning,

10 min of acetone, 1 min of isopropyl alcohol, 1 min of methanol and 2 min of deionized water (D.I. water) were used in this order. Second, the cleaning was carried out with acid and base solvent to remove metal and inorganic impurities. For acid and base solvent cleaning, 10 min of  $\text{H}_2\text{SO}_4 : \text{H}_2\text{O}_2 = 4 : 1$  solution at  $100^\circ\text{C}$ , 10 min of  $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{D.I. water} = 1 : 1 : 5$  solution at  $70^\circ\text{C}$  and 10 min of  $\text{HCl} : \text{H}_2\text{O}_2 : \text{D.I. water} = 1 : 1 : 6$  solution at  $70^\circ\text{C}$ . After cleaning of each solution,  $\text{HF} : \text{D.I. water} = 1 : 10$  solution cleaning was performed for 1 min at room temperature to remove native oxide, and the solution was rinsed for 2 min with D.I. water after each cleaning.

## **3.2 Gate Oxide Deposition and Oxidation**

### **3.2.1 Plasma-enhanced atomic layer deposition system**

A schematic diagram of the PEALD system used in the experiment is shown in the Fig. 3.1. The chamber is divided into a main chamber for deposition and a load lock chamber for loading the sample. A gate valve is used to open and close between the two chambers. There are three source lines, one of which is injected with a Si precursor. The gas line of ALD system has  $\text{O}_2$  and  $\text{N}_2\text{O}$  gas lines for oxidation as well as an Ar line for carrying and purge the ALD behavior. The gas can be regulated from 0 to 500 sccm using a mass flow controller. The main chamber is basically maintained in a vacuum state using a rotary pump, where the base pressure in the chamber is less than  $1 \times 10^{-3}$  Torr.

Temperature of the chamber and lines are individually manipulated, and the temperature of chamber is controlled from 100°C to 350°C. A high frequency power of 13.56 MHz is used for the plasma which power can be adjusted from 100 to 400 W. The plasma is used only for the oxidant pulse time with O<sub>2</sub> gas. The working pressure during deposition is controlled by throttle valve.

### **3.2.2 PEALD conditions of gate oxide deposition**

The conditions of PEALD used for gate oxide deposition are as follows. First, SiH<sub>2</sub>[N(CH<sub>2</sub>CH<sub>3</sub>)<sub>2</sub>]<sub>2</sub> [bis(diethylamino)silane (BDEAS)] was used as a precursor for deposition. The molecular structure of BDEAS is shown in the Fig. 3.2. [71, 72] The BDEAS precursor and Ar carrier gas of 200 sccm were injected into chamber by bubbler type at the source pulse time during the ALD cycle. O<sub>2</sub> plasma was used as the oxidant during oxidant pulse/reaction time, and the plasma power of 200 W was used. The period of source pulse / source purge / oxidant pulse / oxidant purge was 1 / 7 / 2 / 6 sec, respectively. During deposition, the chamber temperature, the gas lines, and the source canister were at 250°C, 100°C, and room temperature, respectively. Pressure was maintained at 3 Torr.

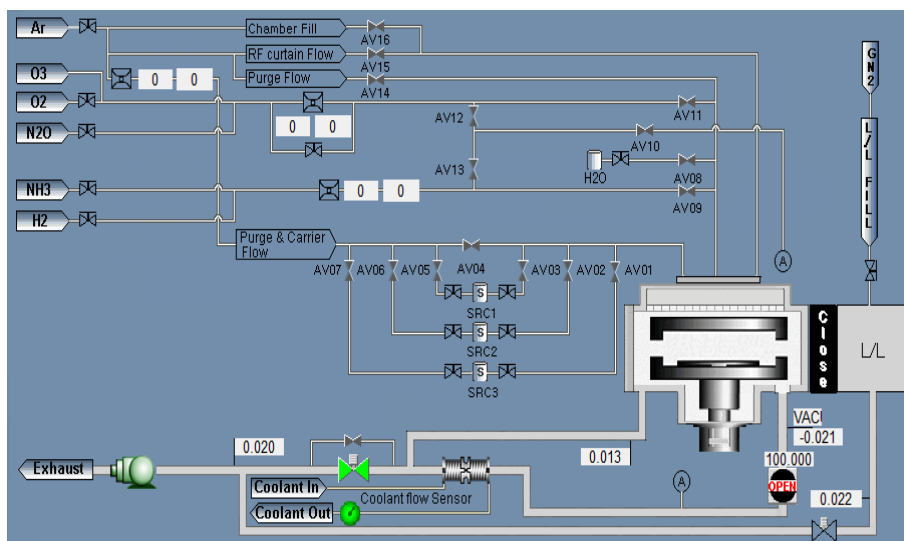


Figure 3.1. A schematic diagram of plasma-enhanced ALD system used in experiment.

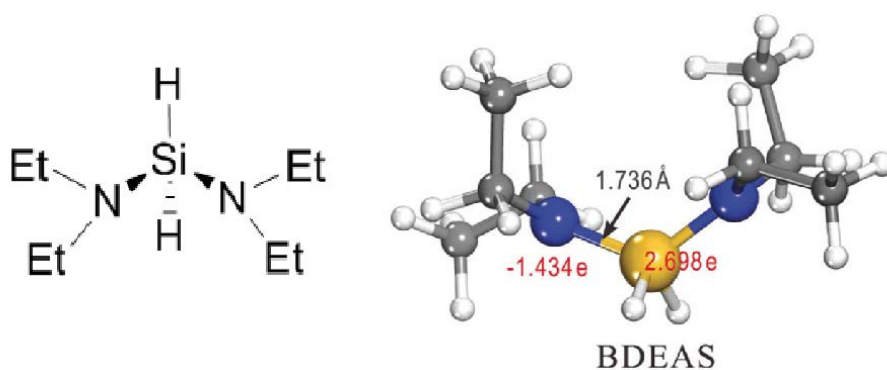


Figure 3.2. Molecular structure of BDEAS precursor

### 3.2.3 Sputtering system and deposition condition

The SiO<sub>2</sub> film was deposited by reactive sputtering. The schematic diagram of sputtering equipment used for deposition is shown in Fig. 3.3. The sputtering equipment consists of a load lock chamber, a transfer chamber and a main chamber. The robot arm is used to move the sample to another chamber. The main chamber was maintained at a base pressure, which was less than  $9 \times 10^{-7}$  Torr for reducing contaminants, using turbo molecular pump. RF power is used for plasma activation during sputtering.

For sputtering of SiO<sub>2</sub>, a pure Si target was used and O<sub>2</sub> was used as an oxidizer gas. During the sputtering, O<sub>2</sub> and Ar were injected at a ratio of 1 sccm : 10 sccm and RF plasma power of 200 W was also applied to the chamber. The sputtering process was performed under a pressure of  $6 \times 10^{-3}$  Torr at room temperature. Before SiO<sub>2</sub> sputtering, pre-sputtering was performed to reduce the contamination of the target.

### **3.2.4 Dry oxidation process**

In order to confirm the relative characteristics of the deposited films, a gate oxide film was formed through dry oxidation. The dry oxidation was conducted at MEMS furnace (Furnace III) of Inter-university Semiconductor Research Center (ISRC) of Seoul National University (SNU), made by Sungjin Semitech Co., Ltd (Model #: JSF-2000-T4). The basic steps of dry oxidation were shown in Fig. 3.4. In experiments, the boat temperature at standard state was 800°C and the dry oxidation temperature was 1080°C. The dry oxidation proceeded to 2, 4, and 12 h depending on the required thickness of 10, 20, and 50 nm, respectively.



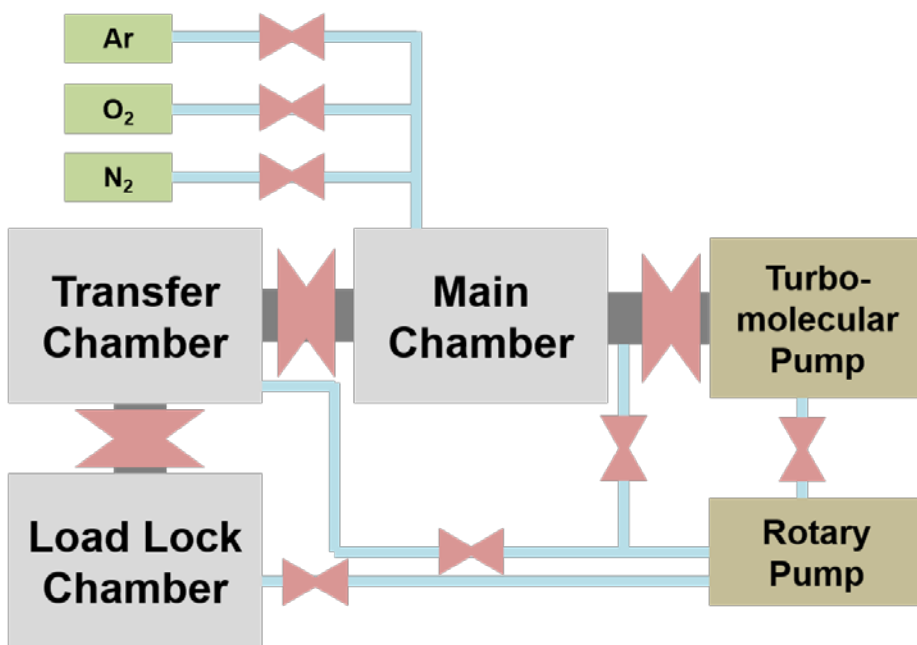


Figure 3.3. A schematic diagram of the sputtering system.

Boat Push	Pre-Heat	Ramp Up	Stabilization	Pre-Oxidation	Dry-Oxidation	Ramp Down	Boat Pull
10 min	10 min	10 min	5 min	3 min	X min	40 min	10 min
N <sub>2</sub> 5000 sccm O <sub>2</sub> 500 sccm	N <sub>2</sub> 5000 sccm O <sub>2</sub> 500 sccm	N <sub>2</sub> 5000 sccm O <sub>2</sub> 500 sccm	N <sub>2</sub> 5000 sccm O <sub>2</sub> 500 sccm	O <sub>2</sub> 7250 sccm	O <sub>2</sub> 7250 sccm	N <sub>2</sub> 5000 sccm	N <sub>2</sub> 5000 sccm

Figure 3.4. Steps of dry oxidation for thermal oxide on 4H-SiC.

### **3.3 Post-deposition annealing process**

#### **3.3.1 Apparatus of furnace for PDA**

A furnace used in the PDA is a hand-made furnace made by Thermotech Co. The heating of the sample takes place in the SiC tube, and vacuum and pressure control are possible during PDA. Available gases for the furnace are Ar, N<sub>2</sub>, O<sub>2</sub>, NH<sub>3</sub>, N<sub>2</sub>O, and NO. In Fig. 3.5, a schematic diagram of the furnace system is shown.

#### **3.3.2 Ar post-deposition annealing**

Post-deposition annealing using Ar gas was conducted to improve characteristics of PEALD oxide. For the Ar PDA, hand-made furnace of Thermotech Co. was used. The temperatures of Ar PDA were 400, 600, 800, 1000, and 1200°C. All samples of Ar PDA were annealing at 20 Torr during 2 h.

### **3.3.3 NO post-deposition annealing**

The NO PDA was performed to improve the deposited oxide characteristics by nitridation. For the NO PDA, hand-made furnace of Thermotech Co. was also used. Since NO gas is classified as dangerous gas, the gas cabinet and leak alarm were separately installed. The temperatures of NO PDA were 1200°C at 400 Torr. during 2 h. Basic NO PDA characteristics were 120 min of annealing time on ALD oxide. On sputtered oxide, The NO PDA were conducted at 30, 60, 90, and 120 min.

### **3.3.4 N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub> Post-deposition annealing**

The sputtering oxide was annealed using N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO gas after deposition. NO PDA utilized the 2 h (120min), 1200°C condition in Chap. 3.3.3. Other PDAs were also carried out for 2 h at 1200°C in hand-made furnace of Thermotech Co. The pressures of N<sub>2</sub> and O<sub>2</sub> PDA were 400 Torr and NH<sub>3</sub> PDA were 4.3 Torr.

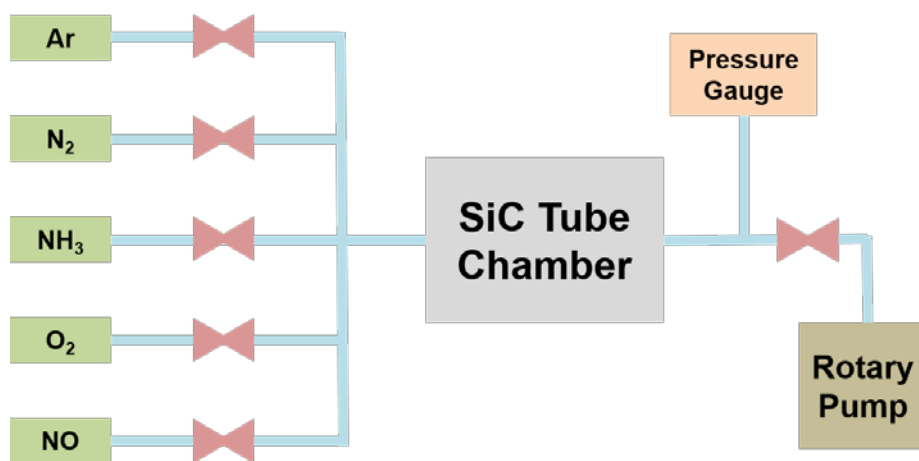


Figure 3.5. A schematic diagram of the furnace system.

### 3.4 MOS Capacitor Fabrication

MOS capacitors were fabricated for electrical evaluation after gate oxide deposition and annealing. All MOS fabrication proceeded at ISRC of SNU. In the case of the gate metal, nickel (Ni) having a work function of 4.6 eV was used, and the Ni was deposited by e-beam evaporation at room temperature. Then, AZ5214 as photoresist was coated by spin coater, and the gate pattern was fabricated through the classic photolithography using MA6-II aligner. After photolithography, the Ni was etched with a solution of sulfuric, nitric, and acetic acid. The remaining PR was removed with acetone. The gate area of all capacitors was  $1.3 \times 10^{-3} \text{ cm}^2$  which was measured optical microscope.

After gate metal deposition, the samples underwent back contact deposition for the Ohmic contact of the substrate. Before back contact deposition, native oxide of the back substrate was removed by buffered oxide etchant (BOE). At this time, the photoresist was coated on the front surface in order to protect the front gate and the oxide film from the BOE. After etching of native oxide by BOE, aluminum (Al) was deposited by thermal evaporation without post-metallization annealing. And then remaining photoresist was removed by acetone. Finally, indium (In) was attached to the side of the sample by a soldering machine for the probe contact of the back contact.

## 3.5 Measurement and Analysis

### 3.5.1 Physical and chemical analysis of gate oxide

The thickness of the deposited oxide film was measured by spectroscopic ellipsometer (M-2000, J. A. Woollam Co., Inc.). The spectroscopic ellipsometer measured at three incident angles of 65°, 70° and 75°, and the spot size of the ellipsometer was about 10 mm in the diameter of longitudinal direction. The ellipsometry analysis was used to determine not only the thickness but also the refractive index.

X-ray photoelectron spectroscopy (XPS) analysis was used to identify chemical bonds. The XPS analysis was commissioned by National Center for Inter-University Research Facilities (NCIRF) of Seoul National University. The x-ray source was monochromatic *Al-K $\alpha$*  of 15 kV, 100 W, 400  $\mu\text{m}$  and vacuum level was  $1.5 \times 10^{-9}$  Torr at x-ray on state.

### 3.5.2 Electrical properties measurement of MOS capacitor

The electrical characteristics of the MOS capacitor were measured using two types of  $C$ – $V$  analyzer and *current-voltage* ( $I$ – $V$ ) analyzer. In the case of the  $C$ – $V$  analysis, a HP4194A analyzer (HP Development Company, L.P., Palo Alto, CA, USA) was mainly used, but a 4200–SCS analyzer (Keithley, Cleveland, OH, USA) was also used to secure the reliability of the measuring device. The  $C$ – $V$  analysis was basically carried out by a double sweep method which reciprocates the sweep. In most cases, it was measured in the direction starting from the inversion region then going back to the inversion and depletion region through the accumulation region. To confirm the oxide capacitance ( $C_{ox}$  or  $C_{max}$ ), the voltage of upper limit was 6 V or more. The measured voltage step is 0.1 V, and the measurement had a delay of 100 ms or more. The measured AC voltage amplitude was 25 mV and the measured frequency was from 1 kHz to 1 MHz. 1 MHz results were only shown when there was no significant difference among measuring frequencies.

HP4140D, HP4155A (HP Development Company, L.P.) and the 4200–SCS analyzer were used for  $I$ – $V$  measurements. The measured  $I$ – $V$  results were converted to units and used as  $J$ – $E$ . The relationships between  $I$  and  $J$ ,  $V$  and  $E$  are as following Eq. 3.1 and Eq. 3.2;

$$J = \frac{I}{A} \quad \text{Eq. 3.1}$$

$$E = \frac{V}{t_{ox}} \quad \text{Eq. 3.2}$$

$A$  is the area of the gate metal, and  $t_{ox}$  is the thickness of the gate oxide film. In case of temperature control in  $J$ – $E$  measurements, samples were placed on hot

chuck and heated. The  $J$ - $E$  measurements were carried out with increasing voltage until the electrical breakdown of gate oxide was confirmed, and the measurement was terminated when the compliance current of 100 mA was reached.

The interface defect density was also extracted by conductance method using a  $C$ - $V$  analyzer. The conductance method was measured with the HP4194A instrument for analysis, and once again with 4200-SCS instrument for reliability. The conductance, which is a secondary value, was extracted using parallel mode ( $C_p$ - $G$  mode). The  $C$ - $\omega$  graph was obtained by sweeping the frequency for each gate voltage at intervals of 0.1 V, and the gate voltage used in the measurement was converted to the energy level of the interface state.



## Chapter 4. Results and Discussions

### 4.1 Characteristics of PEALD Oxide with PDA

#### 4.1.1 Effects of Ar PDA

PEALD has the advantage of being able to react through the plasma with substances with a faster deposition rate and less reactivity than conventional ALD. However, the PEALD SiO<sub>2</sub> films using the BDEAS precursor were difficult to apply to the device because of its poor electrical characteristics if it is not subjected to the subsequent PDA under various deposition conditions. Therefore, the experiments for the optimization of the subsequent PDA process were carried out. The optimum PDA temperature was investigated by using Ar gas, which is an inert gas, to apply pure thermal effects without any other effect.

Etching test was carried out using diluted HF solution to confirm stability of Si–O chemical bonding and density of PEALD deposited 50nm-thick-SiO<sub>2</sub> films. The thermal oxides grown by dry oxidation were also tested for comparison. *Etched thickness–etching time* plots of PEALD oxides with various annealing temperature are shown in Fig. 4.1. During 4 min of etching time, the etched thickness was small in the order of thermal oxide, 1200°C, 1000°C, 800°C, 600°C PDA oxide. As-deposition oxide and 400°C PDA oxide were fully etched during 3 min in HF, which means that 400°C Ar PDA can hardly dense deposited-oxide. The Ar PDAs at 600°C and 800°C are also

incomplete judging from etching rate, but the etching rates of the oxide after 1000°C and 1200°C Ar PDA almost equate to the thermal oxide. As a result, it can be seen that densification of SiO<sub>2</sub> occurs effectively at 1000°C or higher in Ar ambient.

The roughness and RMS values of the etched oxide film surface were measured by AFM, and the results are shown in Fig. 4.2. Bare 4H-SiC and thermal oxide made by dry oxidation at 1270°C were also measured for comparison with Ar PDA samples. The RMS value of dry oxidized oxide surface was larger than that of Bare Si, which is due to residual carbon defect such as carbon clusters. On the other hand, the RMS values of deposited oxide surface with 400–1200°C Ar PDA were maintained at a level similar to the RMS value of the bare 4H-SiC surface. Not only the RMS values of 400–600°C Ar PDA with high etch rate, but also 1000–1200°C Ar PDA shown similar etch rate to those of thermal oxide were significantly lower than the RMS value of dry oxidized oxide. This supports the assumption that carbon defects do not form without O<sub>2</sub> reaction.

*J–E* characteristics of MOS capacitor with PEALD oxide supported the etching test. The *J–E* characteristics of PEALD oxide after various Ar PDA temperature are shown in Fig. 4.3. Measurements were taken at temperatures of 25, 45, 65, 85, 105, and 125°C for all samples. The thickness of the Ar PDA samples was 50 nm, and as-dep sample was 30 nm. Depending on the shape of *J–E* curve, oxide can be classified into three states:

i) The as-deposition case and the cases of Ar PDA below 600°C showed high leakage current density level at all electric field before breakdown. Also, the amount of current depended on temperature below 4 MV/cm. Taken

together, these results suggest that Poole-Frenkel emission occurred in the oxide after Ar PDA below 600°C. This means that there are bulk traps in the oxide, and when compared with the etch results, imperfect Si–O bonds act as bulk traps.

ii) After PDA at 800°C, the leakage current of oxide was significantly reduced. This could be a beneficial phenomenon, but the leakage current increases above 7 MV/cm. In the etching results, the oxide after 800°C PDA had not yet been completely densified, so there would still be multiple traps in the 800°C PDA sample. Therefore, it can be concluded that electrons were filled in the trap site of the oxide, but it did not flow to the gate. Rather, shielding the gate voltage resulted in lower leakage current.

iii) The Ar PDAs at 1000 and 1200°C are another form of  $J$ – $E$  curve. Below 4 MV/cm, it depended on the temperature slightly, but the leakage current was low. Above 4 MV/cm, the leakage current increases, but there is no dependence of PDA temperature, which is considered that leakage current due to F-N tunneling is dominant.

$C$ – $V$  characteristics analysis were conducted to identify the oxide trap. In Fig. 4.4,  $C$ – $V$  and  $G$ – $V$  characteristics of PEALD oxide with Ar PDA at 400, 600, 800, 1000, and 1200°C, respectively. As expected, the oxide after 400°C PDA showed very large  $C$ – $V$  hysteresis due to many bulk traps. After 600 and 800°C PDA, the  $C$ – $V$  curves were very stretched. The shielding phenomenon by trapped electron mentioned in the  $J$ – $E$  characteristics also applied to the  $C$ – $V$  characteristics. In fact, as the voltage at which the leakage current began to increase in  $J$ – $E$  is shifted, the  $V_{FB}$  of  $C$ – $V$  curve was positive-shifted. In the case of 1000°C, it was slightly different from expected in etching test and  $J$ – $E$

characteristics. Judging from the  $C-V$  curve, the oxide after 1000°C Ar PDA was not fully densified. Compared with 1200°C, the  $C-V$  curve in the depletion region showed stretchout form, and it suggested that there were many oxide traps compared to 1200°C. In conclusion, the Ar PDA was effective at more than 1200°C, and below that, it is not effective.

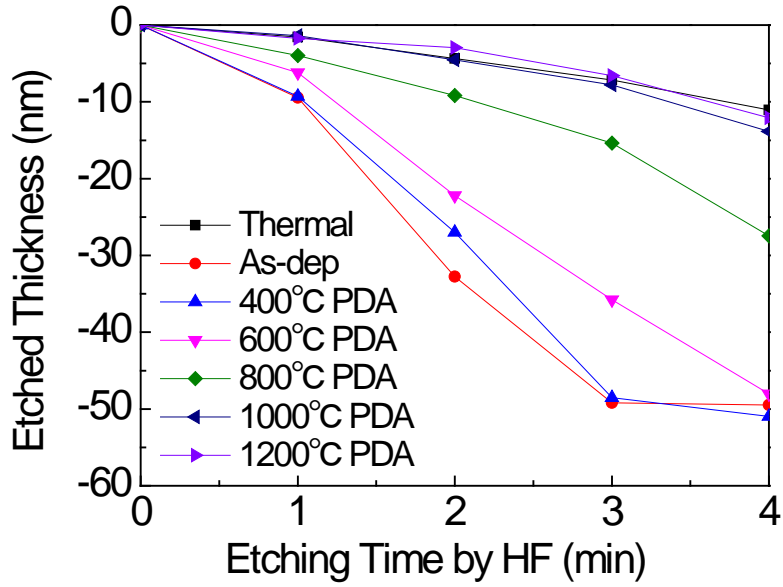


Figure 4.1. Etched thickness of PEALD oxide without and with PDA. Thermal oxide was also etched as reference.

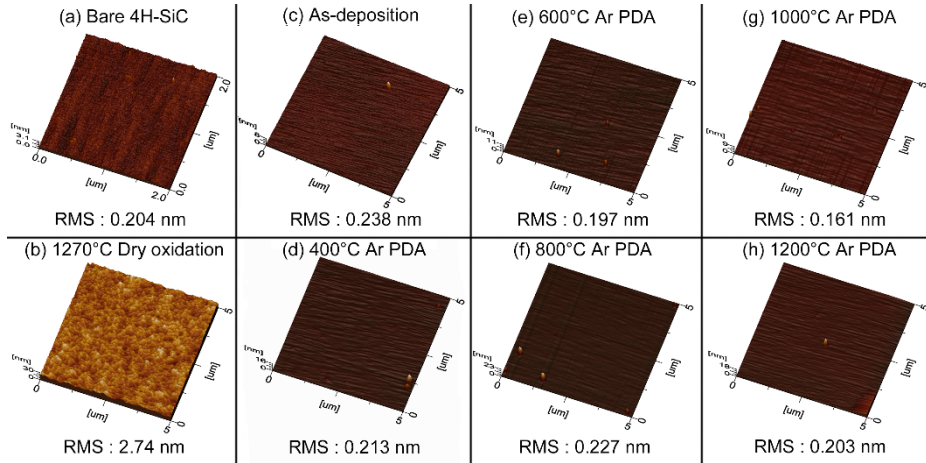


Figure 4.2. AFM images of 4H-SiC surface after SiO<sub>2</sub> etching by diluted HF. The initial surfaces were (a) bare substrate, (b) thermal oxidized SiO<sub>2</sub>, PEALD SiO<sub>2</sub> (c) without and with Ar PDA at (d) 400, (e) 600, (f) 800, (g) 1000, (h) 1200°C, respectively.

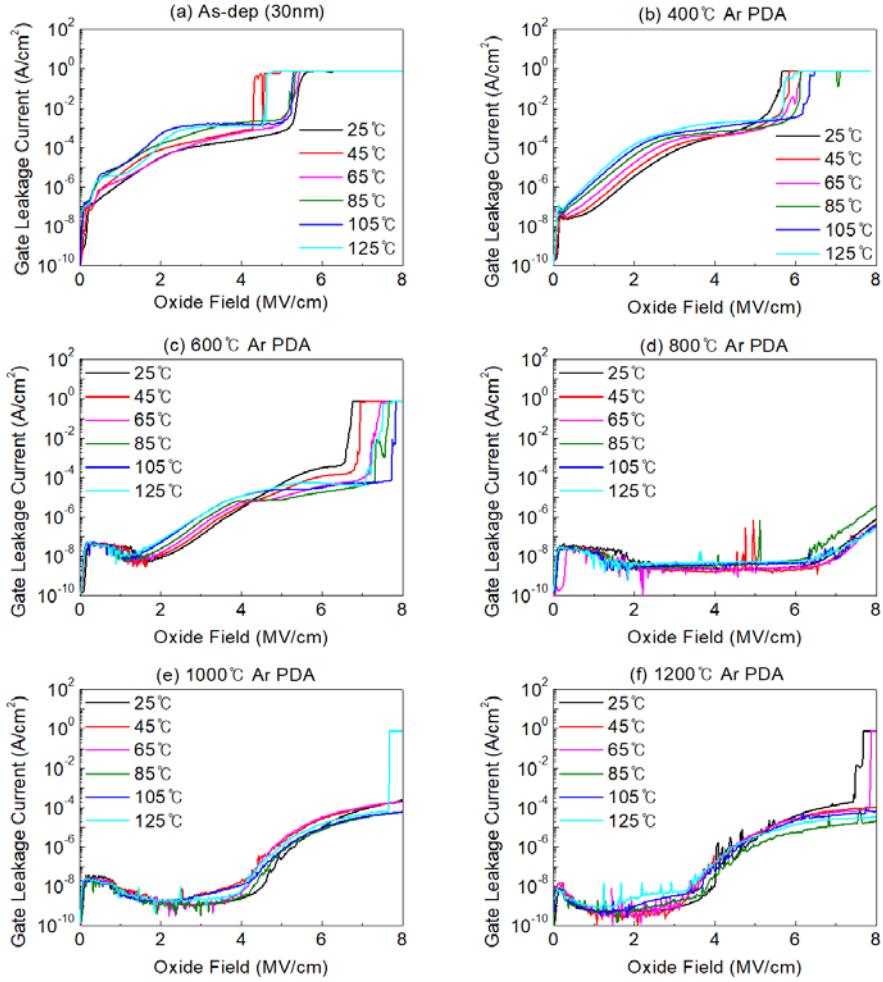


Figure 4.3.  $J$ - $E$  characteristics of PEALD oxide (a) without PDA and with Ar PDA at (b) 400 (c) 600, (d) 800, (e) 1000, and (f) 1200°C, respectively. Each measurement was conducted at 25, 45, 65, 85, 105, and 125°C, respectively.

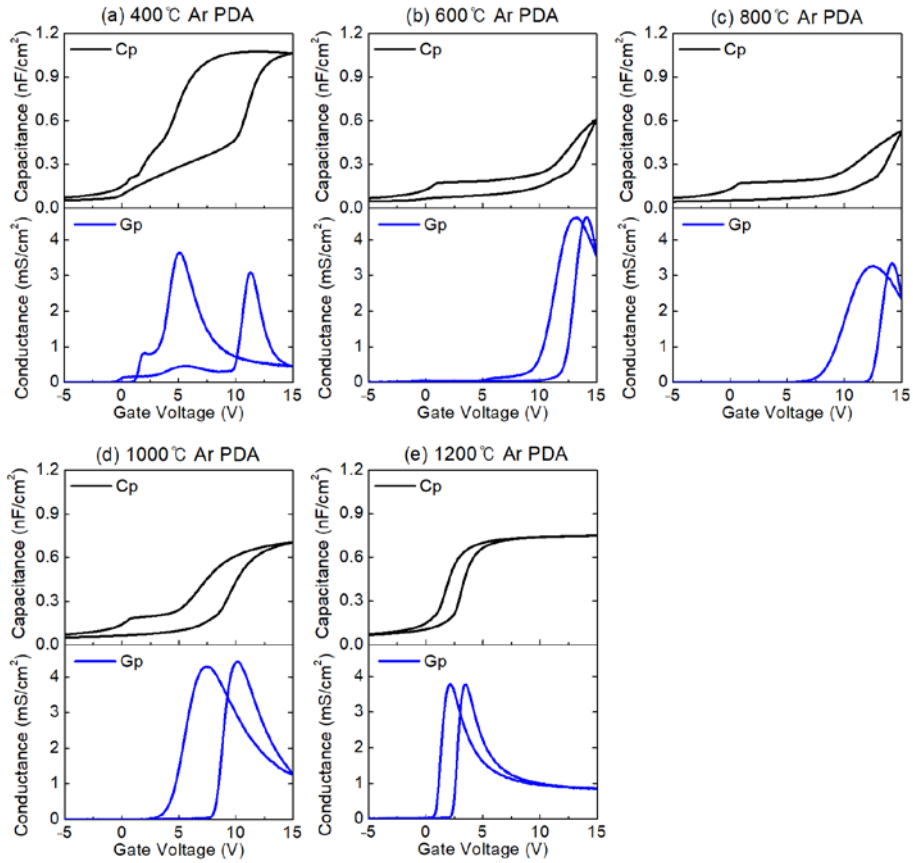


Figure 4.4.  $C$ - $V$  and  $G$ - $V$  characteristics of PEALD oxide with Ar PDA at (a) 400, (b) 600, (c) 800, (d) 1000, and (e) 1200°C.

#### 4.1.2 Effects of NO PDA on 50nm SiO<sub>2</sub>

The results for NO PDA are well reported in Dr. Kim's reports. [13, 65] In this reports, the thickness of deposited gate oxide is as thin as about 30 nm. As the thickness of gate oxide in the commercial device is estimated to be about 70 nm, it is necessary to evaluate the thicker thin film. In the case of thermal ALD, the deposition time is significantly long and it is difficult to deposit a thick oxide. However, PEALD has a relatively fast deposition rate and can deposit thick films in short time.

$C$ - $V$  characteristics of MOS capacitor with 50 nm-thick-oxide are shown in Fig. 4.5. The  $C$ - $V$  sweep was performed with a double sweep, which was a range of  $-2$  V to  $8$  V and then back to  $-2$  V. Without NO PDA, the MOS capacitor was stretched without showing normal  $C$ - $V$  characteristics. This is because that there are many trap of bulk oxide, which is not formed stable chemical bonding. After NO PDA, When comparing the results with the 30 nm-thick-oxide of Fig. 2.28(b), it can be seen that the hysteresis is reduced to almost zero. However, the  $V_{FB}$  of 50 nm-thick-oxide is  $-0.93$  V after NO PDA.  $\Delta V_{FB}$  is related with oxide charges as shown Chap. 2.3.1 and Eq. 2.4. The negative  $\Delta V_{FB}$  represented that positive charges trapped in oxide. Generally, nitridation such as NO, N<sub>2</sub>O or N<sub>2</sub> POA is believed to incorporate positive charges in oxide. [73, 74] Fig. 2.28(b), the result of C. Kim et al., also have same tendency, but  $V_{FB}$  is still positive. There are two factors for the more positive charge of the 50 nm-thick-oxide. First, the C. Kim et al.'s ALD oxide was deposited by thermal ALD using O<sub>3</sub> oxidant. Thermal ALD could produce less bulk oxide than PEALD. Second, more charges may have penetrated as thicker.



Auger electron spectroscopy (AES) analysis was conducted to determine the N concentration by NO PDA, and the results are shown in Fig. 4.6. However, N atoms were not detected by AES analysis. This is because N atoms were not contained in the oxide enough to be detected by AES analysis. The detection range of AES is known to be larger than  $10^{18} \text{ cm}^{-3}$  of bulk concentration, which corresponds to  $10^{12} \text{ cm}^{-3}$  of surface. [75] The molar mass of hexagonal SiC is 40.1 g/mol and the density is 3.16 g/cm<sup>3</sup>. Therefore, the atomic density of SiC is  $4.74 \times 10^{22} \text{ cm}^{-3}$ , so there is less than about 0.01% N atoms. On the other hand, it is known that penetrated N mainly exists at the interface of SiO<sub>2</sub>/SiC after NO POA or PDA. From this AES analysis, it can be seen that there is almost no N atoms or N-related bonds in the bulk oxide when NO PDA is applied on ALD oxide.

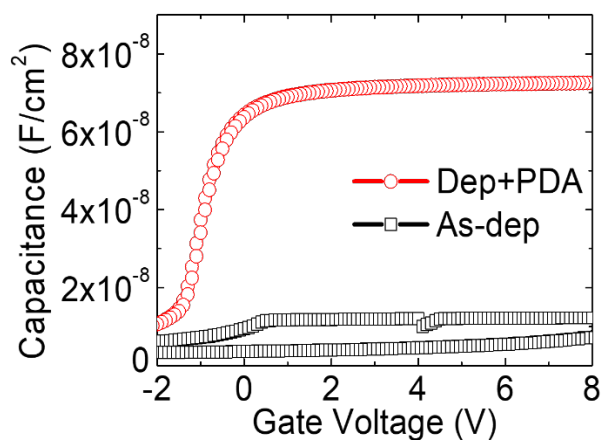


Figure 4.5.  $C$ - $V$  characteristics of MOS capacitors with 50 nm-deposited  $\text{SiO}_2$ . The PDA was operated at  $1175^\circ\text{C}$  for 2 h using NO gas.

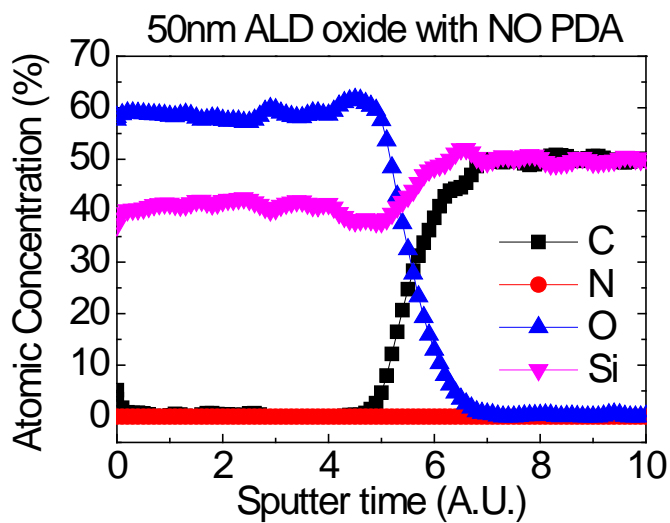


Figure 4.6. Auger electron spectroscopy (AES) results of ALD oxide with NO PDA.

## 4.2 Characterisitscs of Sputtered Oxide with PDA

SiO<sub>2</sub> for gate oxide was deposited by reactive sputtering. We also observed changes in characteristics through PDA. The experiments were described in Chap. 3.2.3 for sputtering and Chap. 3.3.3 and 3.3.4 for PDA by various gases. Through this experiment, I tried to evaluate the applicability of sputtering thin film as gate oxide.

### 4.2.1 Physical and chemical properties

Physical and chemical properties of sputtered SiO<sub>2</sub> on 4H-SiC were investigated. [76] The thickness and refractive index were measured using spectroscopic ellipsometry. The refractive index and thickness ( $t_{ox}$ ) of SiO<sub>2</sub> before and after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA are listed in Table 4.1. The N<sub>2</sub>, NH<sub>3</sub>, and NO PDA decreased  $t_{ox}$  by 17, 27, and 17% compared with a non-treated sample. The O<sub>2</sub> PDA increased slightly  $t_{ox}$  due to oxidation. For the cases of N<sub>2</sub> and NH<sub>3</sub> PDA, it is presumed that some part of the Si, which was not chemically bonded with O, dissociated from SiO<sub>2</sub> at high temperature. Si–N bonds were revealed by X-ray photoemission spectroscopy (XPS) and were attributed to strong N radicals inherent in NH<sub>3</sub> PDA that broke Si–O bonds to form Si–N bonds. In contrast, after O<sub>2</sub> PDA,  $t_{ox}$  increased, due to the reaction of the residual Si with O<sub>2</sub> resulting in SiO<sub>2</sub> formation.

For SiO<sub>2</sub> on 4H-SiC after NO PDA, we expected an increase in  $t_{ox}$  due to oxidation. However,  $t_{ox}$  after NO PDA was comparable to  $t_{ox}$  after N<sub>2</sub> PDA

because of a densification of sputtered SiO<sub>2</sub> and coexisting N radicals. Note that the refractive index of as-deposited oxide is 1.51, which is higher than the ideal value of SiO<sub>2</sub>, 1.46. This indicates that the as-deposited oxide is not in the stoichiometric state of SiO<sub>2</sub>. After N<sub>2</sub>, O<sub>2</sub>, and NO PDA, the dissociation or oxidation of residual Si reduced the refractive index to 1.48, 1.47, and 1.47, respectively, which is close to the ideal refractive index of SiO<sub>2</sub>. The N<sub>2</sub> PDA dissociated Si–Si bonds while the O<sub>2</sub> and NO PDA dissociated Si–Si bonds and formed Si–O bonds. The refractive index increased from 1.51 to 1.67, after NH<sub>3</sub> PDA; this value is almost identical to the refractive index of nitrided SiO<sub>2</sub> by NH<sub>3</sub>, [77] indicating that a nitridation reaction occurred on 4H-SiC during NH<sub>3</sub> PDA.

An SiO<sub>2</sub> etching test using dilute HF (0.5% in H<sub>2</sub>O) was performed for analysis; the measured etching rate is shown in Fig. 4.7. A low etching rate indicates a dense film. For comparison, SiO<sub>2</sub> was also grown on 4H-SiC using dry oxidation and the etching rate measured. Compared with other results, the  $t_{ox}$  value of as-deposited SiO<sub>2</sub> immediately decreased after dipping in the etchant due to porous and non-stoichiometric oxides. However, the etching rate of SiO<sub>2</sub> after PDA was reduced significantly, indicating that PDA stabilizes SiO<sub>2</sub> by a densification process and chemical reaction. The etching rate of SiO<sub>2</sub> after PDA was slightly higher than that of grown SiO<sub>2</sub> by dry oxidation. The thickness reduction of SiO<sub>2</sub> over time by HF dipping had a linear relationship with etching time. However, the etching rate of SiO<sub>2</sub> after NH<sub>3</sub> PDA increased as it went inward from the surface; it is likely that SiO<sub>2</sub> after NH<sub>3</sub> PDA is an unstable oxynitride rather than a stable silicon nitride.

For analysis of the chemical bonding at the SiO<sub>2</sub>/4H-SiC interface, XPS

was conducted using monochromatic Al K $\alpha$ . Si 2p and N 1s spectra were recorded. The SiO<sub>2</sub> on 4H-SiC after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA was etched using dilute HF (1% in H<sub>2</sub>O). The etching time of SiO<sub>2</sub> after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA was 155, 155, 510, and 360 s, respectively, because the  $t_{ox}$  of each sample was different. The remaining SiO<sub>2</sub> thickness was 5 nm for the samples of N<sub>2</sub> and NH<sub>3</sub> PDA after etching. The thickness of SiO<sub>2</sub> in the samples using O<sub>2</sub> and NO PDA was 7 nm. The measured XPS data were aligned to the peak of the 4H-SiC substrate. [78] Si 2p and N 1s spectra of the samples after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA is shown in Fig. 4.8. Chemical bonding in each peak was analyzed based on the literature. [42, 46, 70, 78, 79] After N<sub>2</sub> and NH<sub>3</sub> PDA, the resulting samples showed an Si–N peak, while the sample after O<sub>2</sub> PDA did not. This confirms that N<sub>2</sub> and NH<sub>3</sub> PDA formed silicon nitride (SiN<sub>x</sub>) at the interface, as evidenced by the N 1s spectrum. On the other hand, the thickness of SiO<sub>2</sub> can affect the shoulders of the XPS spectra and distort the intensity of SiN<sub>x</sub>. Our group has reported that the SiN<sub>x</sub> was detected on the deposited SiO<sub>2</sub>/4H-SiC after NH<sub>3</sub> PDA by using secondary ion mass spectrometry. [13] Similar results were also found in the Si 2p spectrum of SiO<sub>2</sub>/4H-SiC after microwave N<sub>2</sub> plasma post-oxidation annealing. [46] The sample after NH<sub>3</sub> PDA exhibited a higher intensity than that after N<sub>2</sub> PDA in the N 1s spectrum. Nitridation was not detected on the sample after NO PDA, and the spectrum of the sample after NO PDA was similar to that of the sample after O<sub>2</sub> PDA. Jamet et al. reported that the Si 2p spectrum of the SiO<sub>2</sub>/4H-SiC after NO annealing exhibited SiO<sub>x</sub>N<sub>y</sub>; [42] however, SiO<sub>x</sub>N<sub>y</sub> or Si<sub>3</sub>N<sub>4</sub> on SiO<sub>2</sub>/4H-SiC after NO PDA was not observed in the samples in this study. This may be caused by the difference between sputtering and oxidation for SiO<sub>2</sub> formation.

Table 4.1. Thickness and refractive index at 632.8 nm of the SiO<sub>2</sub> on 4H-SiC before and after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA.

Samples	Thickness (nm)		Refractive index at 632.8 nm	
	Before	After	Before	After
	annealing	annealing	annealing	annealing
As-dep.	47.04	-	1.51	-
N <sub>2</sub> PDA	46.90	38.80	1.51	1.48
NH <sub>3</sub> PDA	46.43	33.70	1.51	1.67
O <sub>2</sub> PDA	45.19	47.38	1.51	1.47
NO PDA	45.46	38.90	1.52	1.47

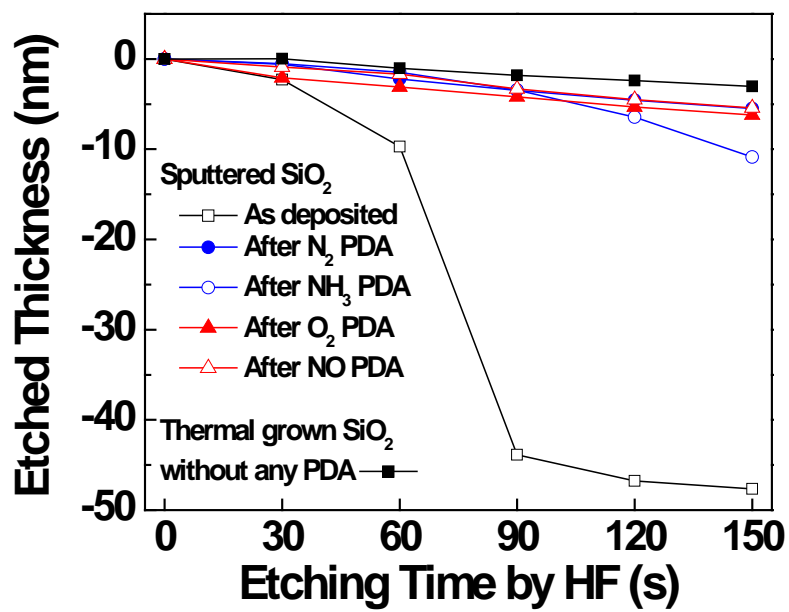


Figure 4.7. Etching rate of the SiO<sub>2</sub> on 4H-SiC before and after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA by dilute HF.

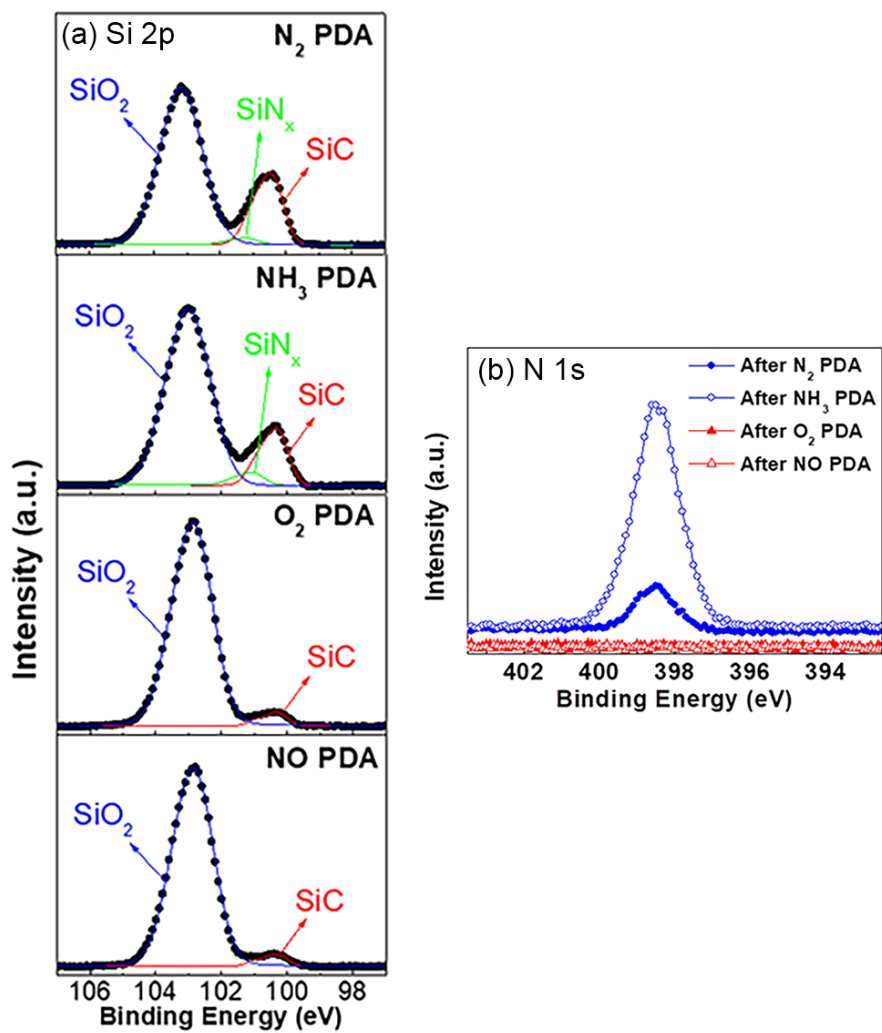


Figure 4.8. (a) Si 2p and (b) N 1s XPS spectra of the SiO<sub>2</sub>/4H-SiC after N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub> and NO PDA.



#### 4.2.2 *J-E* and oxide breakdown characteristics

The *J-E* and time-zero dielectric breakdown (TZDB) characteristics of SiO<sub>2</sub>/4H-SiC MOS capacitors were measured to investigate the electrical characteristics. Fig. 4.9 and Fig. 4.10 show the *J-E* curves and breakdown fields of 20 devices, respectively. The breakdown voltage was strictly defined at the leakage current density of 10<sup>-6</sup> A/cm<sup>2</sup>. The solid point between two bars in Fig. 4.10 indicates the average breakdown field between the maximum and minimum values. The SiO<sub>2</sub>/4H-SiC MOS without any PDA showed poor insulation and a low breakdown field of 0.41 MV/cm; the leakage current of devices was increased by N<sub>2</sub> and NH<sub>3</sub> PDA. The average breakdown fields of devices after N<sub>2</sub> and NH<sub>3</sub> PDA were 0.12 and 0.17 MV/cm, respectively, which is less than the breakdown field of virgin devices. When PDA is conducted in an O-free atmosphere, the residual Si atoms and O-deficient states are likely to remain; in this state, O vacancies can provide leakage current paths in SiO<sub>2</sub>. In addition, the leakage current of the device after N<sub>2</sub> and NH<sub>3</sub> PDA tends to increase sharply because the incomplete oxynitride film is defective. In contrast, the devices after O<sub>2</sub> PDA showed a low leakage current, stable insulating characteristics, and a high breakdown field of 4.71 MV/cm. When PDA was performed under an O<sub>2</sub> atmosphere, the O<sub>2</sub> reacted with residual Si atoms at high temperature; proper insulating characteristics were obtained with the formation of stable SiO<sub>2</sub>. When NO PDA was applied, the leakage current before breakdown was good, but the breakdown field was limited to 3 MV/cm, which can be attributed to the effect of oxide charges. The breakdown field distribution can be further improved by optimizing the fabrication process,

compared with thermally grown SiO<sub>2</sub>. [57]

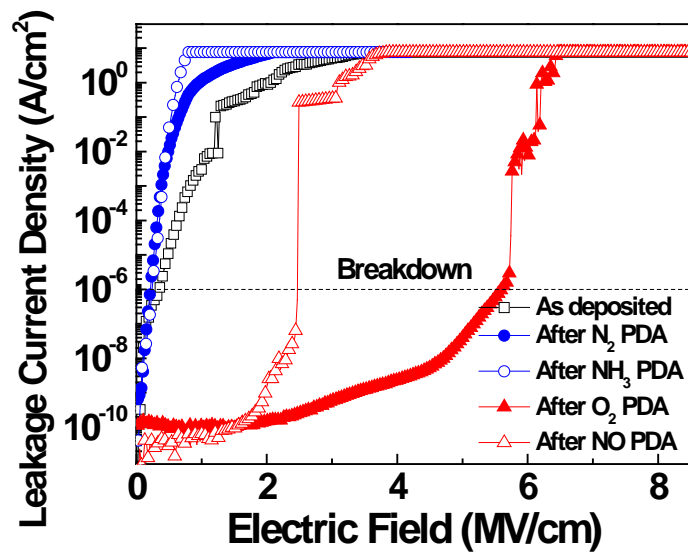


Figure 4.9. Gate leakage current density of the SiO<sub>2</sub>/4H-SiC MOS capacitors using N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub> and NO PDA.

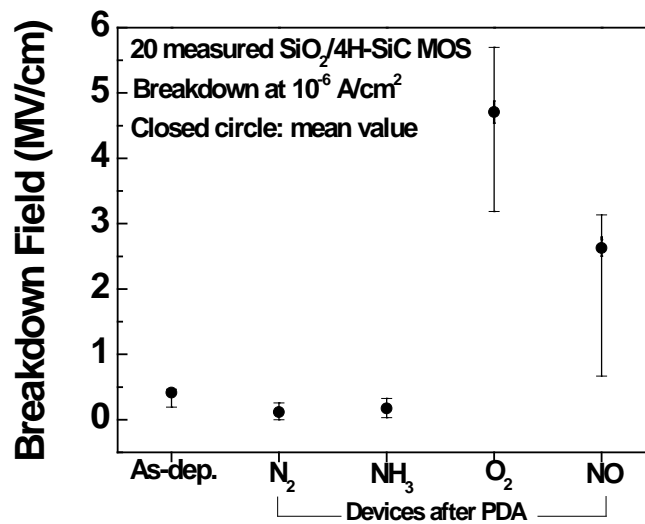


Figure 4.10. Breakdown field of the SiO<sub>2</sub>/4H-SiC MOS capacitors using N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub> and NO PDA.

### 4.2.3 C–V and Dit characteristics

C–V characteristics were measured to extract an  $Q_{\text{eff}}$ ; [52, 80] the capacitance of devices after  $\text{N}_2$  and  $\text{NH}_3$  PDA could not be measured due to the high leakage current. Fig. 4.11 shows the measured C–V characteristics of devices after  $\text{O}_2$  and NO PDA. The capacitance was normalized based on accumulation capacitance, and the theoretical flat-band voltage was 1.35 V. The  $C_{\text{ox}}$  of the devices after  $\text{O}_2$  and NO PDA were  $6.93 \times 10^{-8}$  and  $8.44 \times 10^{-8} \text{ F/cm}^2$ , respectively. The device after  $\text{O}_2$  PDA exhibited a gradual C–V slope and a voltage hysteresis of 0.43 V, which indicates a high interface state density of  $\text{SiO}_2/\text{4H-SiC}$ . [49] The shift in the flat-band voltage ( $\Delta V_{\text{FB}}$ ) of the device after  $\text{O}_2$  PDA was 0.95 V. The  $Q_{\text{eff}}$  was extracted from the  $\Delta V_{\text{FB}}$  value of the C–V characteristics. In  $Q_{\text{eff}}$  extraction, the right-side C–V curve was used, which is expected to be trapped during the C–V sweep. The  $Q_{\text{eff}}$  of the device after  $\text{O}_2$  PDA was  $-4.11 \times 10^{11} \text{ cm}^{-2}$ , indicating that negative charges are trapped at interface states. In contrast, the voltage hysteresis of the device after NO PDA was small with suppressed interface states; however,  $V_{\text{FB}}$  was strongly shifted in the negative direction by  $-2.56 \text{ V}$ . The  $Q_{\text{eff}}$  of the device after NO PDA was high, at  $1.11 \times 10^{12} \text{ cm}^{-2}$ . The sputtered  $\text{SiO}_2/\text{4H-SiC}$  after 2 h-long NO PDA exhibited the negative  $V_{\text{FB}}$  of  $-2.56 \text{ V}$  while the ALD  $\text{SiO}_2/\text{4H-SiC}$  after the same PDA showed the positive  $V_{\text{FB}}$  of  $1.36 \text{ V}$ . [65] This is caused by the difference of deposition technology. The sputtered oxide is more porous than the ALD oxide. The optimization of NO PDA can change  $V_{\text{FB}}$  of the sputtered  $\text{SiO}_2/\text{4H-SiC}$  to the ideal value.

C–V was also measured with the wide range of voltage, and the results are

shown in Fig. 4.12. The voltage was applied from 8, 10, 12, 14, or 16 to  $-6$  V for the device after  $O_2$  PDA, and from 6, 8, 10, or 12 to  $-6$  V for the device after NO PDA. It is noted that the breakdown voltage of the device after NO PDA was about 10 V. The  $V_{FBS}$  were negatively shifted slightly for the higher starting voltage in both cases, and the larger shift was shown in the case of NO PDA. It means that both oxides are charged and the device after NO PDA contains more charges. The oxide charges can contribute the leakage current and breakdown.

Fig. 4.13 exhibits the measured  $D_{it}$  of  $SiO_2/4H-SiC$  MOS after  $O_2$  and NO PDA. The  $D_{it}$  was extracted by the conductance method.  $D_{it}$  of devices after  $O_2$  and NO PDA were  $4.1 \times 10^{12}$  and  $2.5 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$  at 0.1 eV of  $E_c-E_t$ , respectively. The  $D_{it}$  after NO PDA was slightly less than that of after  $O_2$  PDA at shallow level, but  $D_{it}$  of NO PDA dropped significantly at deep level. The  $D_{it}$  of  $O_2$  PDA was almost similar to that of thermal oxide. This trend is consistent with the slope and hysteresis of the  $C-V$  curve. NO or  $N_2O$  PDA has been also reported in the literature to improve the  $C-V$  characteristics and  $Q_{eff}$  of ALD  $SiO_2/4H-SiC$  MOS. [65, 68] In other words, although the  $O_2$  PDA stabilized the sputtering oxide, the interfacial characteristic was deteriorated due to the oxidation process. However, the NO PDA exhibited better interface characteristic due to stabilization by O atoms and nitridation by N atoms.

The improvement of the sputtered  $SiO_2/4H-SiC$  by  $O_2$  and NO PDA was caused by the densification and additional oxidation. This oxidation formed the oxide layer with better quality to the sputtered  $SiO_2$ . Also, the  $SiO_2/4H-SiC$  interface was redefined to be between grown  $SiO_2$  and  $4H-SiC$ . The densified sputtered  $SiO_2$  have still several issues when applying to the power device fabrication, such as low breakdown field and high-density oxide charges. The

time of N<sub>2</sub>, NH<sub>3</sub>, O<sub>2</sub>, and NO PDA was fixed at 2 h in this work, although the time for NO PDA was longer than the optimum condition for sputtered SiO<sub>2</sub> on 4H-SiC. The optimization of PDA and suppression of pinholes in the oxide can improve the electrical characteristics of the sputtered SiO<sub>2</sub>/4H-SiC MOS.

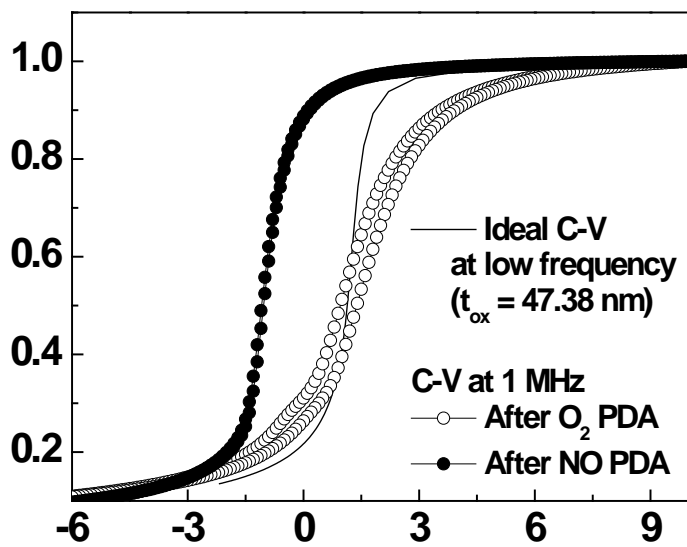


Figure 4.11. C-V characteristics of the SiO<sub>2</sub>/4H-SiC MOS after O<sub>2</sub> and NO PDA.

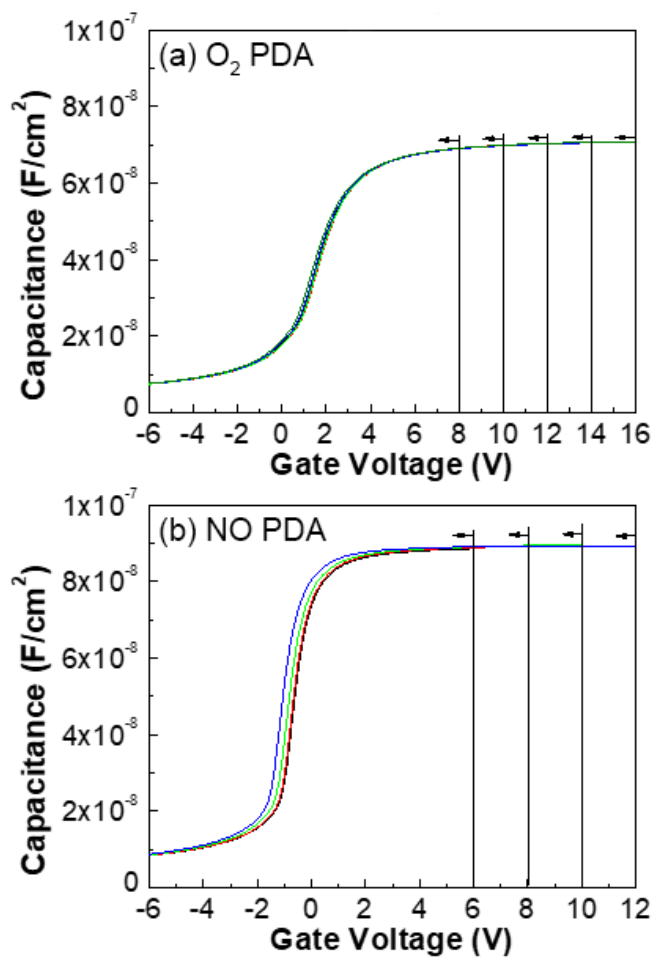


Figure 4.12.  $C$ - $V$  characteristics of the  $\text{SiO}_2/4\text{H-SiC}$  MOS after  $\text{O}_2$  and NO PDA with different start voltage. The arrow indicates the start voltage.



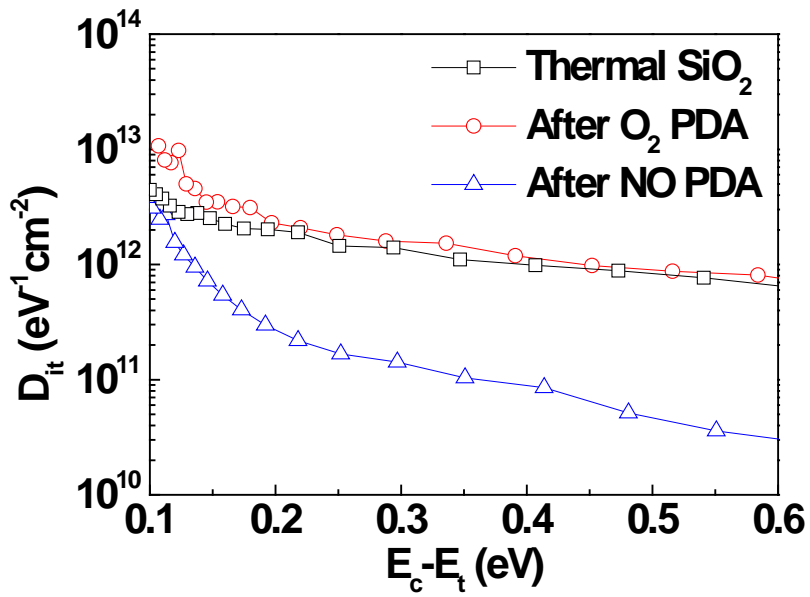


Figure 4.13.  $D_{it}$  of the  $\text{SiO}_2/4\text{H-SiC}$  MOS after  $\text{O}_2$  and NO PDA. For comparison,  $D_{it}$  of thermal  $\text{SiO}_2$  is also shown.

## 4.3 Analysis of Sputtered Oxide with NO PDA

### 4.3.1 $C$ - $V$ curve analysis

Fig. 4.14 shows the  $C$ - $V$  characteristics of the fabricated  $\text{SiO}_2/4\text{H-SiC}$  MOS capacitors. The voltage swept from depletion ( $-4$  V) to accumulation (6 V) and back in Fig. 4.14(a), and from accumulation to depletion and back in Fig. 4.14(b). The flat band voltage ( $V_{\text{FB}}$ ), the  $C$ - $V$  hysteresis between  $V_{\text{FB}}$  of left and right  $C$ - $V$  curve of double sweep ( $\Delta V_{\text{hys}}$ ) and the effective oxide charge ( $Q_{\text{eff}}$ ) extracted from each  $C$ - $V$  curve in Fig. 4.14 listed in Table 4.2. Without the NO PDA, normal  $C$ - $V$  behavior could not be confirmed due to the large leakage current. In Fig. 4.14, the longer the NO PDA time, the more  $V_{\text{FB}}$  was shifted negatively. This is due to the positive charging inside the oxide, which is attributed to the diffusion of N atoms. As shown before chapters, the films deposited with ALD show the same tendency. [65] The thickness of thermal oxide tends to increase during NO PDA, but in case of sputtering oxide, densification resulted in reducing  $t_{\text{ox}}$ . After NO PDA for 30 min, the  $C$ - $V$  hysteresis is larger than that of the 60 and 90 min cases and the  $V_{\text{FB}}$  is positive side rather than  $V_{\text{FB}}$  of the ideal curve (1.355 V). This suggests that 30 min-long PDA may not complete the densification. In addition, the 90 min-long PDA shifted  $C$ - $V$  toward a negative direction corresponding with the ideal case, but  $C$ - $V$  hysteresis was greatly reduced. It is assumed that the diffusion of N as positive charge for at least 90 min. Overall, the  $Q_{\text{eff}}$  of 60 min case was the smallest as  $0.35 \times 10^{11}$  and the  $V_{\text{FB}}$  was close to the ideal  $V_{\text{FB}}$ . However, the

smallest value of  $\Delta V_{\text{hys}}$  was 234 mV of 90 min case.

The  $C$ – $V$  hysteresis greatly changes according to the sweep direction of Fig. 4.14(a) and (b). When a double sweep is started from a positive voltage (Fig. 4.14(b)), the left curve of Fig. 4.14(a) appears to move to vicinity of the right curve. In addition, when the device is repeatedly measured after Fig. 4.14(a) result, the shape of the repeated  $C$ – $V$  curve as shown in Fig. 4.14(b). From this result, it can be seen that the trap inside the oxide is filled with the negative charge at accumulation. However, when strong negative voltage stress was applied, the same result like Fig. 4.14(b) was shown. It was confirmed from these results that there was almost no recovery at negative trap site in short term. Generally, electrons trapping is difficult but de-trapping is easy. Therefore, it is difficult to understand this phenomenon. The model is analyzed in the next chapter.

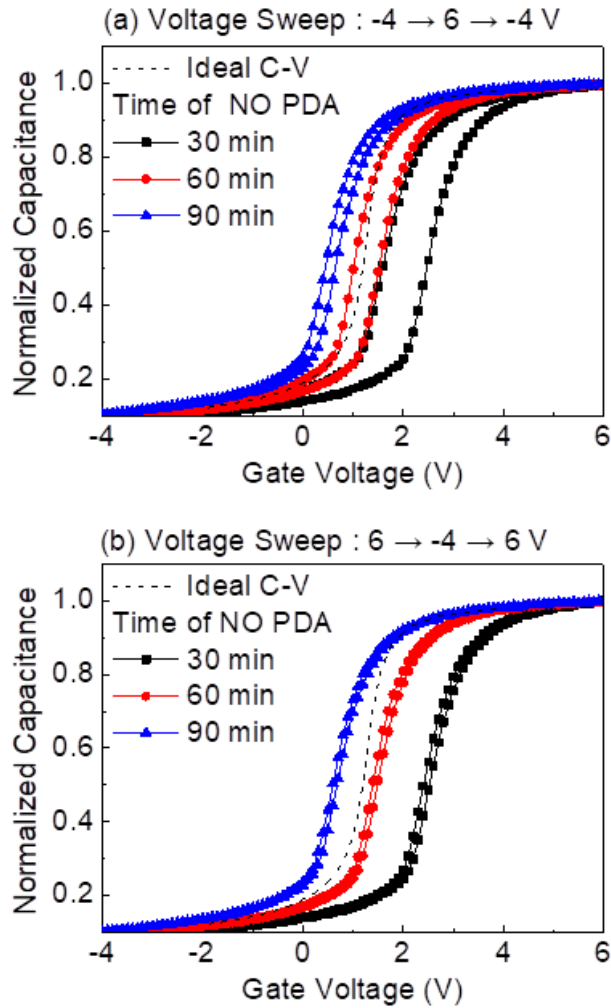


Figure 4.14. C-V characteristics of the SiO<sub>2</sub>/4H-SiC MOS after NO PDA with various annealing time. The voltage swept from depletion (-4 V) to accumulation (6 V) and back in (a), and from accumulation to depletion and back in (b).

Table 4.2. Measured flat-band voltage ( $V_{\text{FB}}$ ),  $C$ - $V$  hysteresis ( $\Delta V_{\text{hys}}$ ), and effective oxide charge density ( $Q_{\text{eff}}$ ) extracted from  $C$ - $V$ . The “L” means left curve and “R” means right curve.

<b>Sample</b>		<b><math>V_{\text{FB}}</math> of <math>L</math></b>	<b><math>V_{\text{FB}}</math> of <math>R</math></b>	<b><math>\Delta V_{\text{hys}}</math></b>	<b><math>Q_{\text{eff}}</math> of <math>L</math></b>	<b><math>Q_{\text{eff}}</math> of <math>R</math></b>
		(V)	(V)	(mV)	( $\text{cm}^{-2}$ )	( $\text{cm}^{-2}$ )
(a)	NO 30'	1.877	2.721	844	$-2.91 \times 10^{11}$	$-7.38 \times 10^{11}$
	NO 60'	1.249	1.758	509	$+0.35 \times 10^{11}$	$-2.32 \times 10^{11}$
	NO 90'	0.684	0.918	234	$+3.30 \times 10^{11}$	$+2.08 \times 10^{11}$
(b)	NO 30'	2.669	2.786	117	$-7.47 \times 10^{11}$	$-8.12 \times 10^{11}$
	NO 60'	1.623	1.732	109	$-1.69 \times 10^{11}$	$-2.29 \times 10^{11}$
	NO 90'	0.851	0.935	84	$+2.54 \times 10^{11}$	$+2.08 \times 10^{11}$

### 4.3.2 Modeling of charging in near interface traps

The model described in the previous chapter is shown in Fig. 4.15. As described, this general electron charging model does not explain the results of negative bias. The near interface traps are filled with electrons like Fig. 4. 15(c), strong negative voltage at gate metal should force the electrons de-trapped. However, applying  $-50$  V during 20 min at gate did not transform  $C-V$  curve. Therefore, another model was considered.

Fig. 4.16 shows another model of explaining why the  $C-V$  hysteresis are different with the direction of the sweep voltage. After deposition or oxidation, positive charges are filled with near interface traps initially, although its origin cannot be specified. In accumulation, these positive charges are de-trapped through the valence band of 4H-SiC. And then, near interface traps remains empty in the proper range of voltage. If there is a strong accumulation voltage, the electron will be trapped. Both Fig. 4.15 and Fig. 4.16 have limitations, but Fig. 4.16 is more suitable for stress characteristics.

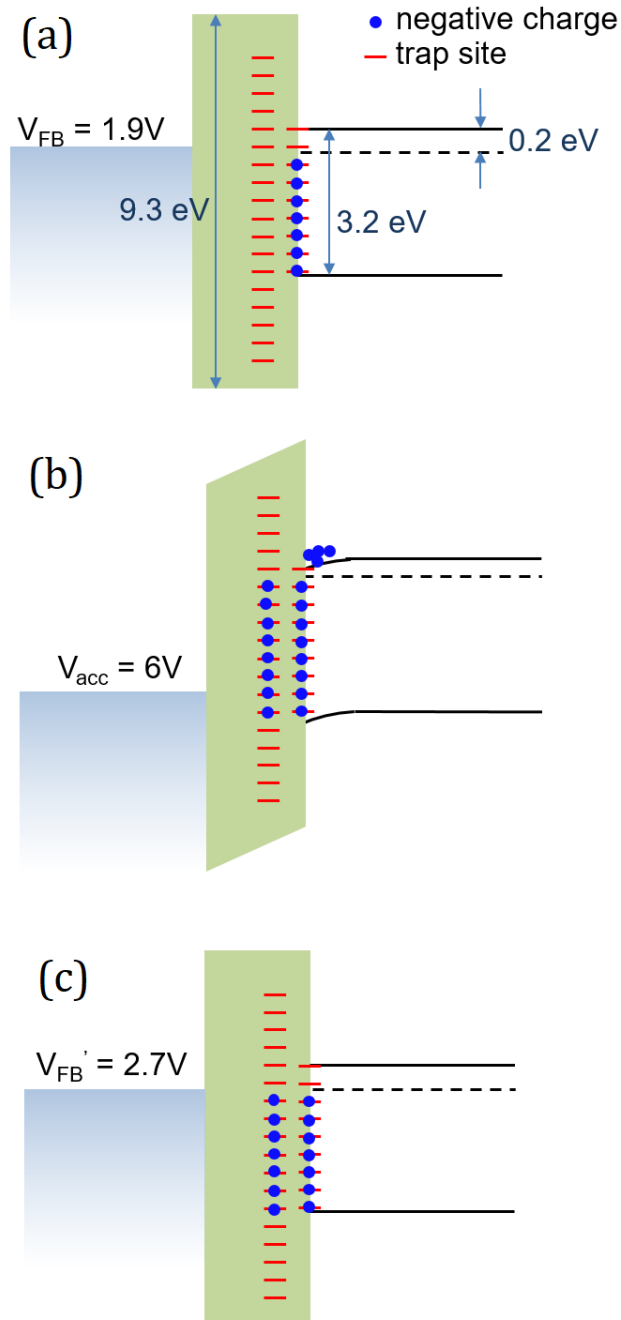


Figure 4.15. Negative charging model at near interface traps when positive voltage applied. (a) Near interface traps are not charged initially. (b) In accumulation, negative charges are trapped in near interface traps. (c)  $V_{FB}$  are shifted to positive by negative charging.

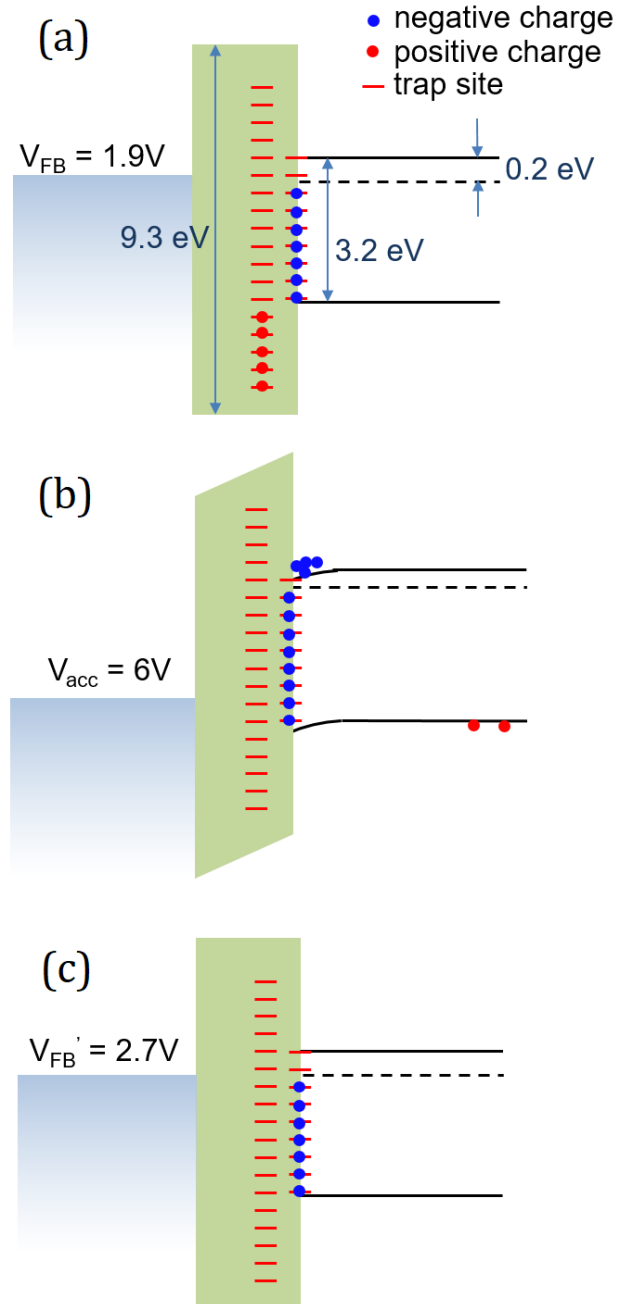


Figure 4.16. Initially positive charging model at near interface traps. (a) Near interface traps are positive charged initially. (b) In accumulation, positive charges are de-trapped in near interface traps. (c)  $V_{FB}$  are shifted to positive voltage when compared to the initial charging state.



### 4.3.3 $G-\omega$ and $D_{it}$ analysis

In general, the conductance measured in an equivalent parallel circuit is related to the carrier capture and emission of  $D_{it}$  as shown Chap. 2.3.2. Fig. 4.17 shows the  $G_P/\omega$  value of the equivalent parallel circuit calculated from the thin oxide film. the Eq. 2.10 were used to the relations of  $G_P$  and  $\omega$ .

The repeated  $C-V$  sweep was conducted before conductance measurements to charging of oxide trap. As  $E_c - E_t$  decreasing, the overall conductance value increases, indicating that shallow traps are more dominant than deep traps. The conductance after 30 min-long PDA is higher than that after 60 or 90 min-long PDA for each energy level. This means that the density of interface state after 30 min-long PDA is higher than that after 60 or 90 min-long PDA at the whole range of the frequency. Although there are many noises, similar values are observed in 60 min PDA and 90 min PDA at the shallow level (Fig. 4.17(c)). This indicates that PDA of 90 min rather increased the deep trap, although the effect on the shallow trap was minimal.

Fig. 4.18 shows the  $D_{it}$  extracted by the conductance method.  $D_{it}$  was extracted from maximum conductance using Eq. 2.9. The maximum  $G_P/\omega$  value of the right term in Eq. 2.9 is determined from the peak in Fig. 4.17. Fig. 4.18 shows  $D_{it}$  extracted in the range of  $10^3$  Hz to  $10^6$  Hz. Above  $10^6$  Hz, the sharply increasing peaks exist, which will be discussed in Chap. 4.5. The amount of the interface state near the conduction band edge is similar for each sample, but the interface state of 30 min PDA case is 1.5 ~ 2 times higher than other cases above 0.3 eV. In addition, there are more deep traps at 90 min PDA case compared to 60 min as already shown in Fig. 4.17, which seems to be due to excessive

nitridation. The result that the shallow trap did not decrease as the annealing time increased was a feature of sputtering oxide. Assuming that the film was deposited at room temperature to suppress oxidation and there was almost no residual carbon, the NO gas reaction would take place in a different direction compared with the oxidation. It is also expected that a chemically unstable thin film would be formed in reactive sputtering rather than oxidation. When assuming such an oxide film, a chemically stable oxide formation including densification is preferentially generated instead of a substitution reaction of a carbon cluster in a NO PDA process. Therefore, the NO PDA of sputtered oxide plays a role different from the role of a conventional NO POA, which is removing residual carbon cluster by formation of C–N bond. [81]

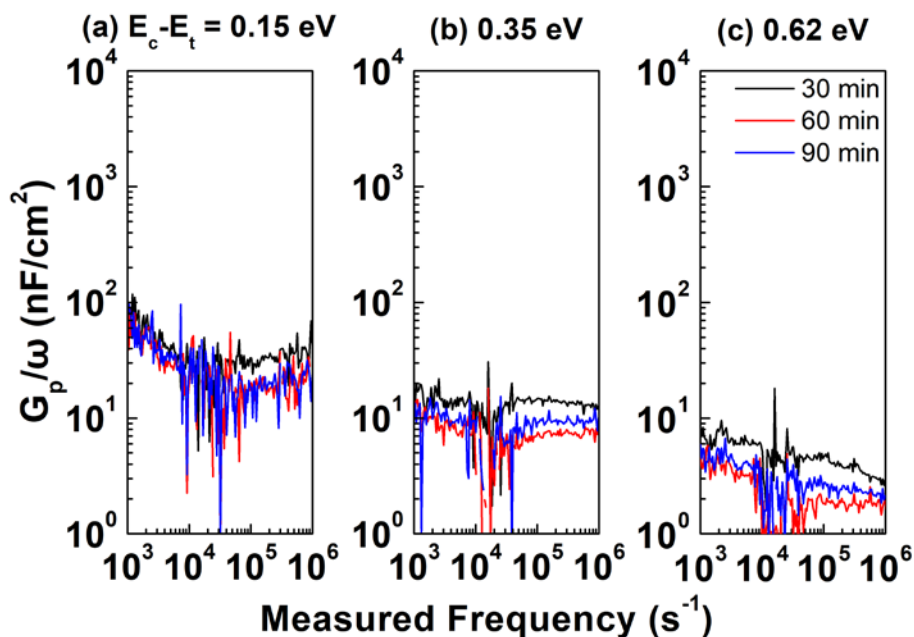


Figure 4.17. Normalized conductance characteristics at different energy levels ( $E_c - E_t$ ) of (a) 0.62 , (b) 0.35 and (c) 0.15 eV.

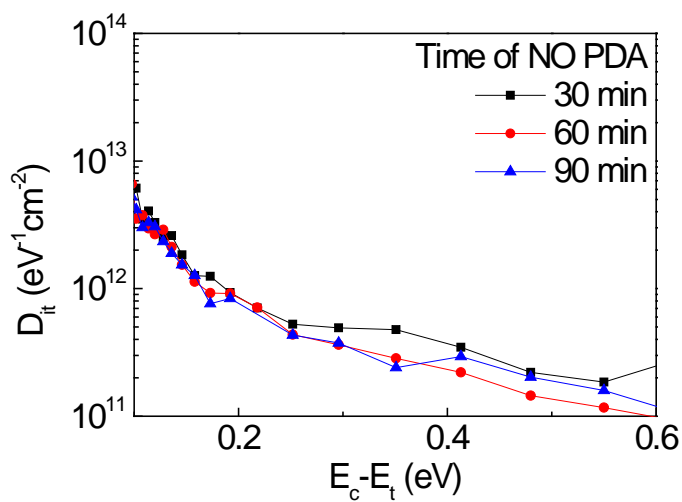


Figure 4.18.  $D_{it}$  distributions as a function of energy level with frequency ranges of  $10^3$  to  $10^6$  Hz.

## 4.4 Deposited Oxide with Thermal Oxide Interlayer

The common point between PEALD and sputtering is that plasma is used, although their purpose is different. When the plasma is used on substrate directly, the substrate could be damaged by the plasma. In the case of oxide films formed by sputtering and PEALD, the oxide without PDA were not able to function as capacitors due to the large leakage current. In consideration of the possibility that this is due to the plasma damage, thin thermal oxide was grown to reduce the damage before deposition, and then the electrical characteristics were evaluated.

### 4.4.1 PEALD oxide with dry thermal oxide

Pre-oxidation was carried out through basic dry oxidation.  $\text{SiO}_2$  with a thickness of 10 nm and 20 nm were formed by dry oxidation for 2 h and 4 h, respectively. After that, the  $t_{\text{ox}}$  was adjusted to about 40 nm by deposition. The calculated capacitance equivalent thickness (CET) and  $t_{\text{ox}}$  were calculated from the measured capacitance in Table 4.3. As the ALD thin film increases, the CET decreases, but it does not differ greatly. It is considered that PEALD oxide is acting as a dielectric. The capacitance is compared in Fig. 4.19. As the thickness of PEALD increases, the hysteresis increases as compared with the thermal oxide of the same thickness. The bulk oxide of PEALD clearly shows that there are many traps.

Frequency dispersion of  $C-V$  were shown in Fig. 4.20 to identify the

interface traps. In Fig. 4.20(a) and (b), the longer the dry oxidation time, the larger the dispersion, which means that the interface traps increased. In the case of dry oxide 10 nm/PEALD oxide 30 nm, frequency dispersion was worse than dry-oxidation, but in case of dry oxide 20 nm/PEALD oxide 20 nm, frequency dispersion was reduced. 10 nm of dry oxide is seemed to be insufficient to mitigate plasma damage. On the other hand, 20 nm of dry oxide can mitigate plasma damage and the interface trap generated by dry oxidation can be minimized.

*J-E* characteristics are also measured, and shown in Fig. 4.21. 27 nm thermal oxide showed more irregular and unstable than 40 nm oxide. 40 nm thermal oxide showed stable characteristics and breakdown occurred after F-N tunneling region. In the cases of dry oxide 10 nm/PEALD oxide 30 nm and dry oxide 20nm/PEALD oxide 20nm, the leakage currents were lower than 40nm thermal oxide. In addition, hard breakdowns occurred suddenly at low current densities in both case. The difference of the curve shape from the thermal oxide indicates that the conduction of leakage currents was different, but it is confirmed that it is a sufficiently usable oxide film as a substitute for thermal oxide.

Table 4.3. Capacitance equivalent thickness (CET) and real oxide thickness ( $t_{ox}$ ) of dry oxidation oxide and pre-oxidized/PEALD oxide.

	CET (nm)	$t_{ox}$ (nm)
<b>Dry oxidation</b>	41.9	40.8
<b>Dry 10 nm + ALD 30 nm</b>	38.2	40.5
<b>Dry 20 nm + ALD 20 nm</b>	37.6	40.7

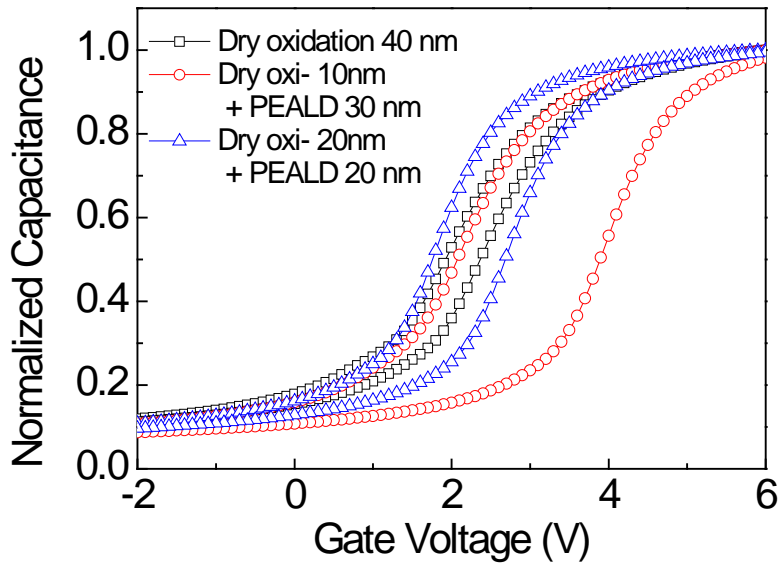


Figure 4.19. Normalized capacitance of dry oxidation oxide and pre-oxidized/PEALD oxide.

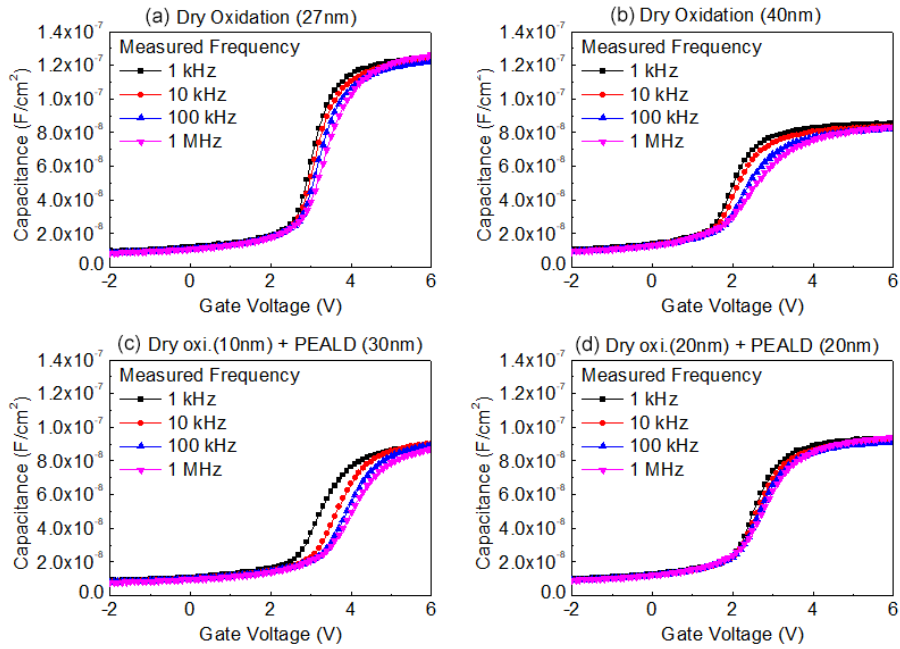


Figure 4.20. C-V frequency dispersion characteristics of (a) 27 nm-thick dry oxide, (b) 40 nm-thick dry oxide, (c) 10 nm-thick dry oxide/30 nm-thick PEALD oxide, and (d) 20 nm-thick dry oxide/20 nm-thick PEALD oxide.

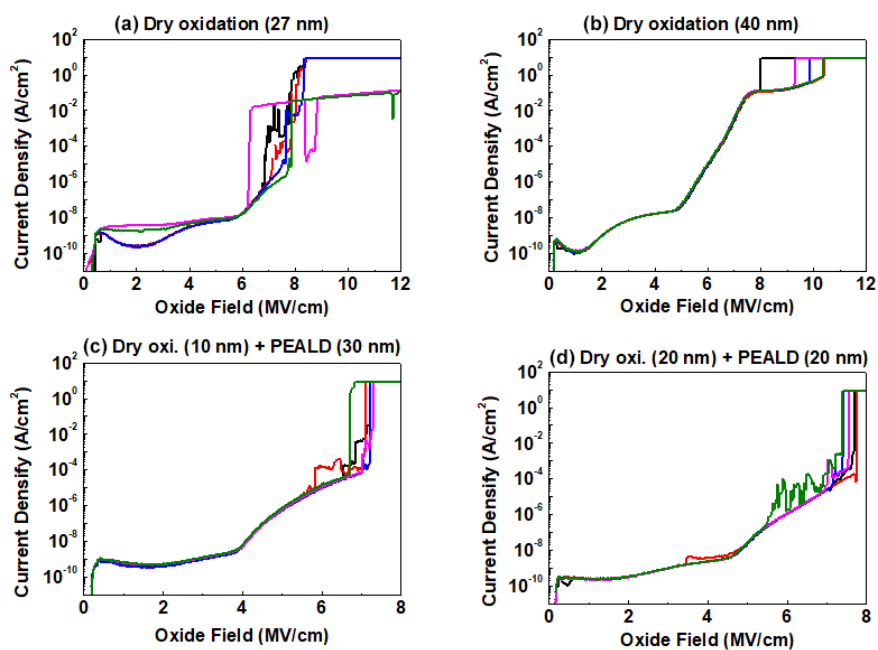


Figure 4.21.  $J$ - $E$  characteristics of (a) 27 nm-thick dry oxide, (b) 40 nm-thick dry oxide, (c) 10 nm-thick dry oxide/30 nm-thick PEALD oxide, and (d) 20 nm-thick dry oxide/20 nm-thick PEALD oxide.



#### 4.4.2 PEALD oxide with NO thermal oxide

It is already known that nitridation of interface through NO gas is effective. In order to utilize this, oxidation was carried out using NO gas and additional oxide film was deposited with PEALD. Fig. 4.22 shows the capacitance of the oxide layer deposited with PEALD after 8 nm and 13 nm of NO-oxidized oxide. Unfortunately, neither of them showed good characteristics. Both have a very large  $C-V$  hysteresis compared to pure dry thermal oxide. It is thought that the oxidation by NO gas only formed more unsafe oxide. The fact that the leakage current at TZDB characteristics in Fig. 4.23 was somewhat small could be an advantage, but breakdown voltage was lower than thermal oxide.

In Chap. 4.1.2, less than 0.1% N atoms significantly improve  $C-V$  characteristics by NO PDA. Direct NO oxidation can incorporate more N atoms in the interface than NO PDA. Therefore, excessive nitridation may have a detrimental effect on the interface properties. N 1s XPS results of O<sub>2</sub> and NO oxidation samples are shown in Fig. 4.24. Compared with O<sub>2</sub> oxidation, there is a peak at 397 eV in NO oxidation. That is, it means that N atoms are contained in the interface enough to be detected by XPS. Similar to AES, XPS has a detection limit of 0.1% in inorganic compound. [82] From this, it can be assumed that more N atoms would have influenced the interface, and it is possible that excessive nitridation caused the  $C-V$  characteristics to deteriorate.

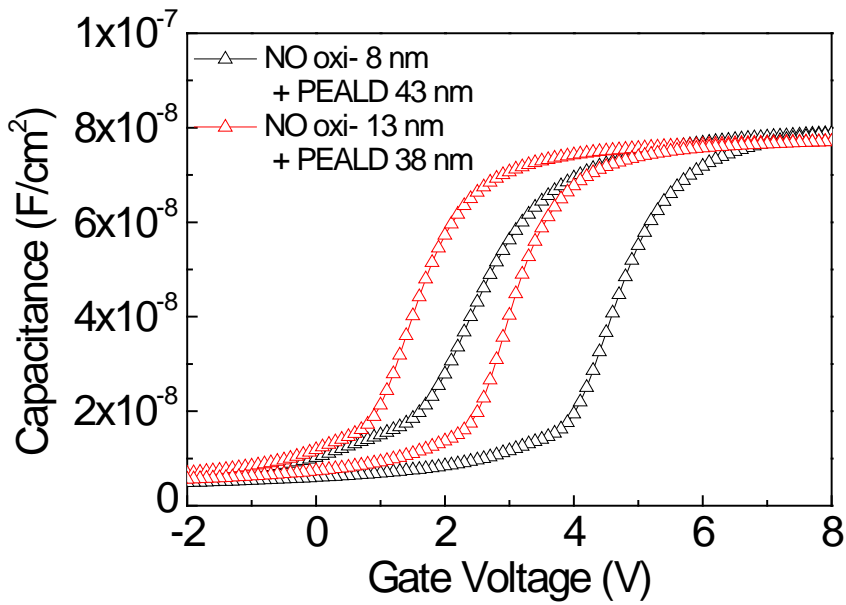


Figure 4.22. C–V characteristics of 8 nm-thick NO-oxidized oxide/43 nm-thick PEALD oxide and 13 nm-thick NO-oxidized oxide/38 nm-thick PEALD oxide.

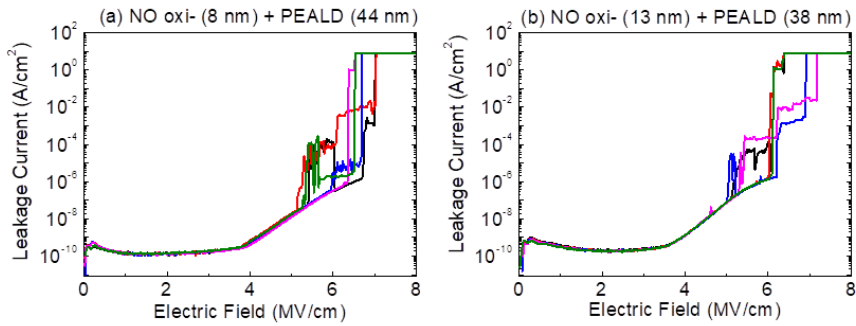


Figure 4.23. TZDB characteristics of (a) 8 nm-thick NO-oxidized oxide/43 nm-thick PEALD oxide and (b) 13 nm-thick NO-oxidized oxide/38 nm-thick PEALD oxide.

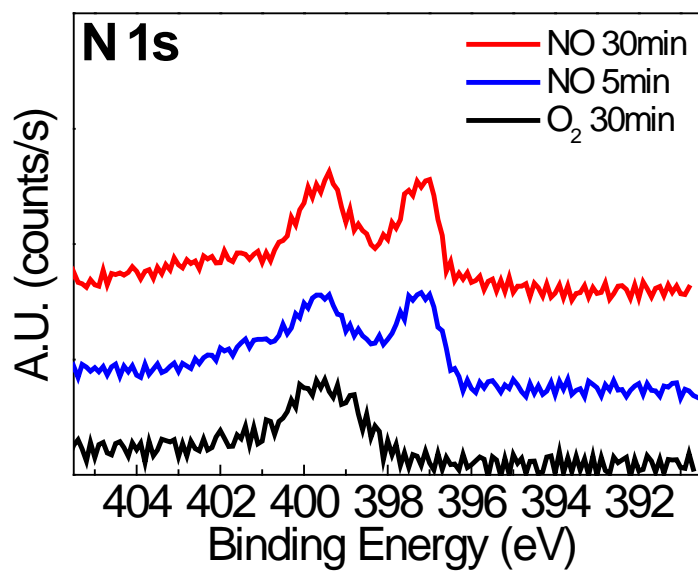


Figure 4.24. N 1s spectra of SiO<sub>2</sub> surface by XPS analysis after O<sub>2</sub> and NO oxidation.

#### 4.4.3 PEALD oxide with NO/O<sub>2</sub> and N<sub>2</sub>O thermal oxide

Since the characteristics of pre-oxide through NO oxidation was not good, pre-oxidation was carried out using NO/O<sub>2</sub> mixed gas and N<sub>2</sub>O gas in order to make oxide film more stable. The fraction of NO/O<sub>2</sub> mixed gas was NO : O<sub>2</sub> = 1 : 10 and 1 : 20. The *C-V* characteristics of NO/O<sub>2</sub>-oxidized oxide are shown in Fig. 4.25. Unlike O<sub>2</sub> and NO pre-oxide, pre oxidation with NO/O<sub>2</sub> mixed gas before PEALD was effective on *C-V* hysteresis and *V<sub>FB</sub>* shift. As have seen, NO oxidation formed incomplete SiO<sub>2</sub> in the oxidation process, and if it is pre-oxidized by dry oxidation, it cannot largely compensate the bulk-oxide characteristics. It is considered that all of the effects can be applied by using a mixture of gases.

N<sub>2</sub>O gas was also used for pre-oxidation and *C-V* characteristics are shown in Fig. 4.26. N<sub>2</sub>O pre-oxidation can also be found to be effective enough to reduce hysteresis. Also, as the pre-oxidation time increases from 30 to 60 min, *V<sub>FB</sub>* shifted to negative, which is confirmed that nitridation effects exist. As a result, N<sub>2</sub>O and NO/O<sub>2</sub> PDA showed the same effect because N<sub>2</sub>O is decomposed into NO and O<sub>2</sub> at high temperature.

However, according to results of XPS analysis in Fig. 4.27 of samples oxidized by N<sub>2</sub>O and NO/O<sub>2</sub> mixed gas, N atoms were not found. The above results showed that N was found in the oxide film which had poor *C-V* characteristics. In conclusion, even if the nitridation effect is seen in *C-V*, trace amounts may be acting so as not to be detected by chemical analysis such as XPS or AES. In addition, these very small amounts of nitridation can make electrical properties superior to excessive nitridation. As mentioned earlier

chapters, the detection ranges of XPS and AES are more than 0.01%. Less than 0.01% of N atoms should be considered effective.

$J$ - $E$  characteristics were measured in Fig. 4.28 and Fig. 4.29 for samples pre-oxidized with NO/O<sub>2</sub> mixed gas and N<sub>2</sub>O. Both cases showed high leakage current and lower breakdown field than thermal oxide. It is presumed that the N atoms, which were improved the  $C$ - $V$  characteristics, deteriorate the  $J$ - $E$  characteristic by charge-induced leakage current characteristics. Interestingly, the more negative the  $V_{FB}$  was in  $C$ - $V$  characteristics, the more current density was shifted toward positive. Since the negative shift of  $V_{FB}$  is a positive charge by N atoms, it cannot be concluded that the N atoms increase the leakage current. It has yet to be clarified causally, but seems to be a need to study further.

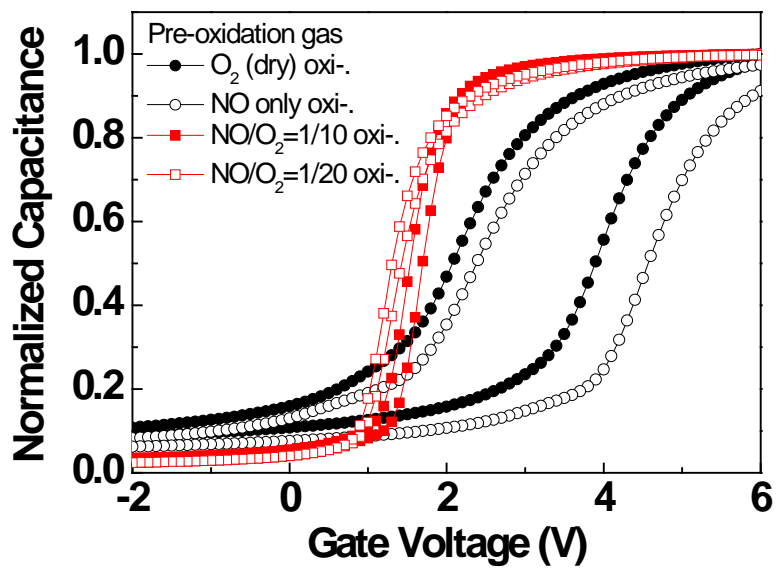


Figure 4.25.  $C$ – $V$  characteristics of  $\text{NO}+\text{O}_2$ -oxidized oxide/PEALD oxide. For comparison,  $\text{O}_2$ -oxidized oxide/PEALD oxide and NO-oxidized oxide/PEALD oxide are also shown.

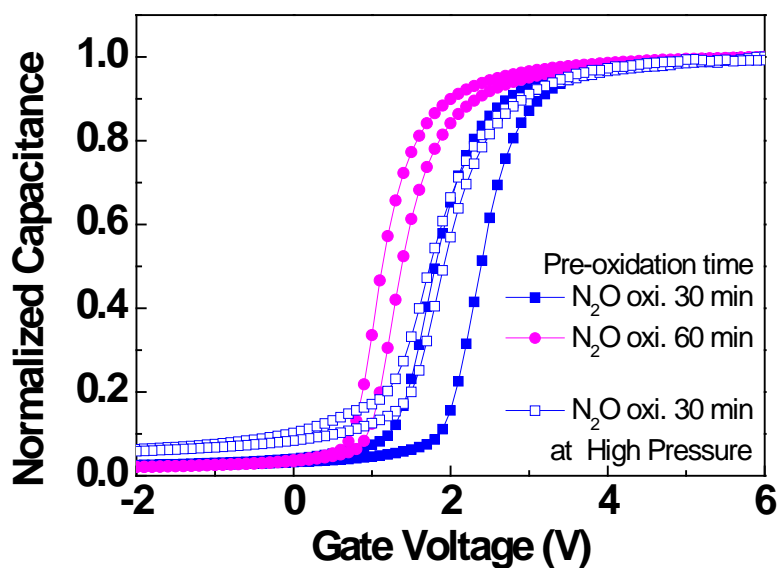


Figure 4.26.  $C$ - $V$  characteristics of  $N_2O$ -oxidized oxide/PEALD oxide.  $N_2O$  oxidation was conducted during 30 and 60 min. High pressure sample was conducted  $N_2O$  oxidation above 760 Torr during 30 min.

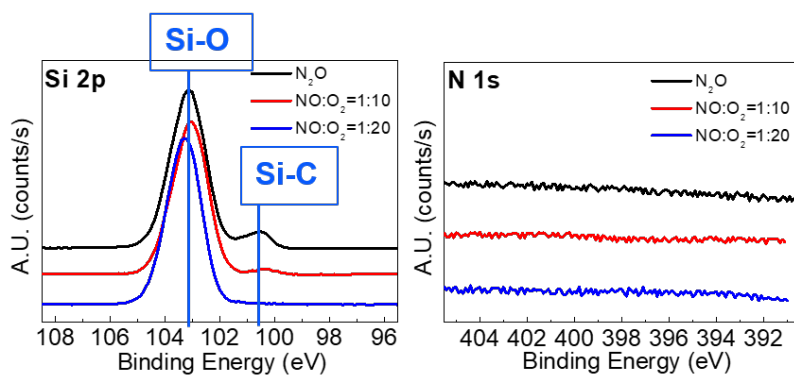


Figure 4.27. (a) Si 2p and (b) N 1s spectra of thin  $N_2O$ -oxidized oxide and  $NO/O_2$ -oxidized oxide in XPS analysis.

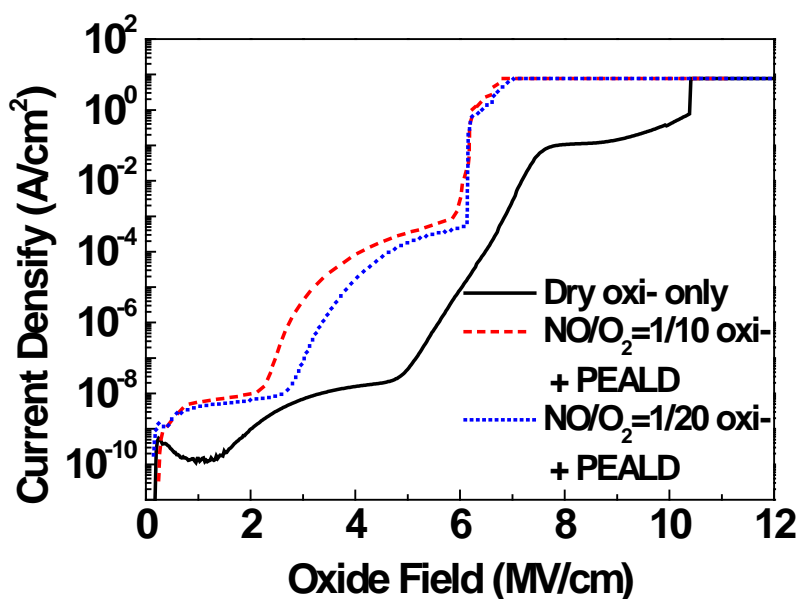


Figure 4.28.  $J$ - $E$  characteristics of  $(\text{NO}+\text{O}_2)$ -oxidized oxide/PEALD oxide. For comparison, dry thermal oxide was also shown.

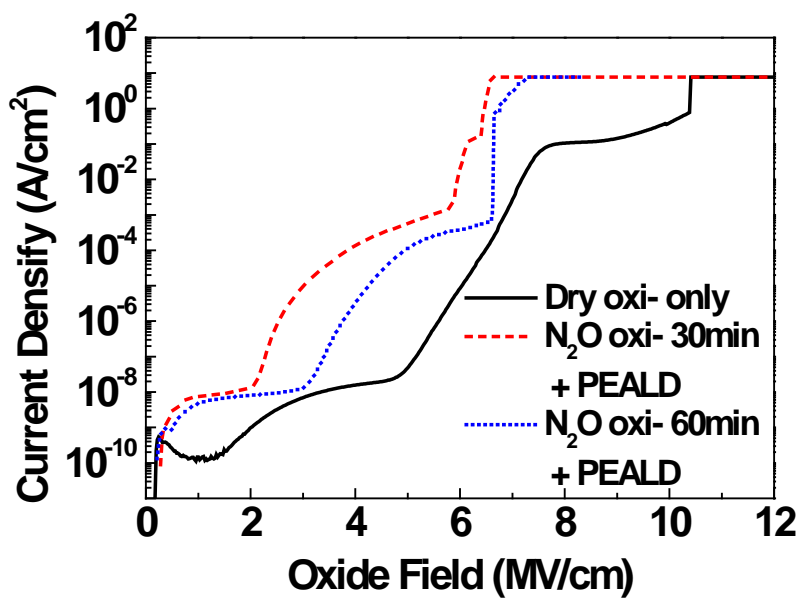


Figure 4.29.  $C$ - $V$  characteristics of  $\text{N}_2\text{O}$ -oxidized oxide/PEALD oxide. For comparison, dry thermal oxide was also shown.



#### 4.4.4 Sputtering Oxide with dry thermal oxide

Sputtering is also a method of depositing using plasma like PEALD. Therefore, it is possible to improve the characteristics of the as-deposited thin film through the buffer layer of the thermal oxide. The pre-oxidation and sputtering stacking results are shown in Fig. 4.30. Unlike PEALD oxide, the  $C-V$  characteristics did not vary greatly depending on the  $t_{ox}$ . It is still noteworthy that the properties are worse than dry thermal oxide, but there are few significant differences depending on thickness. CET and  $t_{ox}$  of samples are shown in Table 4.4. The thermal oxide/sputtering samples showed lower CET than the  $t_{ox}$  measured with ellipsometry, unlike thermal oxide/PEALD samples. The sputtering oxide consists the  $SiO_{2-x}$  state in the as-deposition state more than the PEALD oxide.

$D_{it}$  of pre-oxidized  $SiO_2$ /sputtering  $SiO_2$  are shown in Fig. 4.31. Sputtering oxide with pre-oxidation had a large  $D_{it}$  value in the near conduction band compared with thermal oxide.  $G_p/\omega$  characteristics showed slow traps at  $10^3$  Hz were more sputtering oxide with pre-oxidation than only dry oxidized oxide. Although the experiment was not carried out in this dissertation, I expect that sputtering can be improved by pre-oxidation with  $N_2O$  like PEALD oxide.

$J-E$  characteristics are also shown in Fig. 4.32. Capacitors with thermal oxide/sputtering oxide showed higher leakage current and lower breakdown field than that with thermal oxide only. The thinner the thermal oxide, the poorer the properties, which means the characteristics of sputtering oxides are inferior to those of thermal oxide. Another reason is that the oxide field is calculated by dividing the gate voltage by the thickness of the oxide film. In

fact, the difference between actual  $t_{ox}$  and CET was already confirmed. Therefore, the electric field of the actual oxide film may be larger than that shown. It is true that for some reason the properties are not excellent. However, the expected part is that the leakage current is in the form of thermal oxide. In Chap 4.2.2, the large leakage current was shown in as-deposition sputtering oxide. Therefore, pre-oxidation is helpful for the sputtering oxide film to serve as an insulating film.

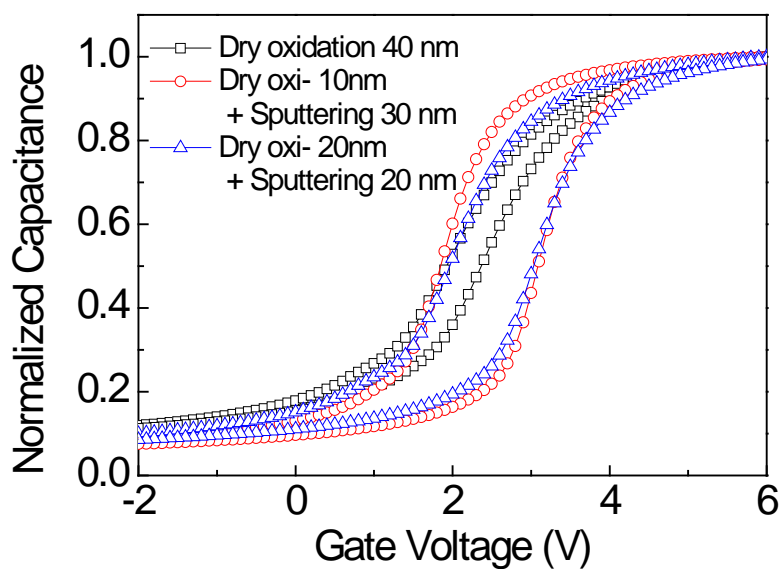


Figure 4.30.  $C$ – $V$  characteristics of dry-oxidized oxide/sputtering oxide.

Table 4.4. Capacitance equivalent thickness (CET) and real oxide thickness ( $t_{ox}$ ) of dry oxidation oxide and pre-oxidized/PEALD oxide.

	CET (nm)	$t_{ox}$ (nm)
<b>Dry oxidation</b>	41.9	40.8
<b>Dry 10 nm + Sputter 30 nm</b>	31.9	39.2
<b>Dry 20 nm + Sputter 20 nm</b>	33.4	39.7

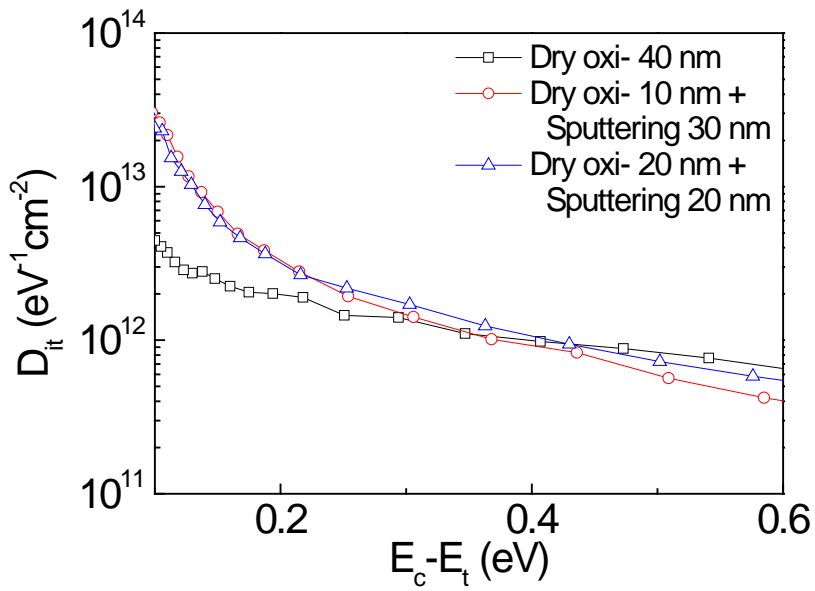


Figure 4.31.  $D_{it}$  of dry thermal oxide/sputtering oxide.

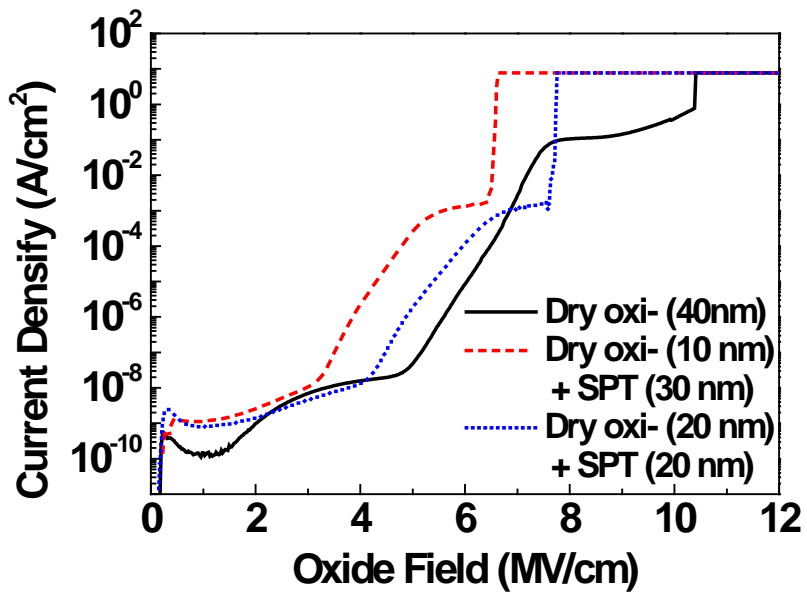


Figure 4.32.  $J$ - $E$  characteristics of dry thermal oxide/sputtering oxide. SPT means sputtering oxide.

## 4.5 Experiments Summary

Gate oxide were formed through PEALD and sputtering with PDA, and characteristics of MOS capacitors on 4H-SiC were analyzed. In order to evaluate the possibility of using oxide film by pure densification on the 50 nm oxide film deposited with plasma-enhanced ALD (PEALD), the PDA was performed using Ar gas, which is an inert gas. At this time, the PDA was operated at 400, 600, 800, 1000, and 1200°C for 2 h. HF etch test and leakage current analysis showed that the oxide film stabilized at 1000°C or higher. However, in the  $C$ - $V$  characteristics, the 1000°C sample was found to be in a less stable state, and a stable oxide film was formed only at 1200°C. In addition, the NO PDA, known to be effective at 30 nm, was conducted for 2 h at 1200°C on PEALD oxide. The  $C$ - $V$  hysteresis decreased significantly compared to as-dep oxide, but the flat-band voltage ( $V_{FB}$ ) shifted significantly in the negative direction. This is because the thicker the oxide film, the greater the nitrogen charging. From these results, it is considered that optimized results on 30 nm-thick-ALD oxide cannot be applied unconditionally to thicker films.

Reactive sputtering oxide with PDA were evaluated. The PDAs were conducted using  $N_2$ ,  $NH_3$ ,  $O_2$ , and NO gas. All the samples were found to have sufficient densification through refractive index and HF test, and in the case of  $O_2$  PDA, an additional oxidation reaction occurred. As a result of the insulation property evaluation,  $N_2$  and  $NH_3$  did not have good insulation characteristics, which seems to be the result of the chemical reaction of nitrogen increasing the leakage current. In the case of  $O_2$  and NO, it showed some insulation

characteristics but it was insufficient compared to thermal oxide. It is considered that pinhole is formed in sputtering and pinhole is caused by leakage current. In addition, it was confirmed that a large amount of positive charge penetrated into oxide at the time of NO PDA in the  $C-V$  characteristic. For the optimization of NO PDA for sputtering oxide, the 30, 60, and 90 min of NO PDAs were also investigated. As PDA time increased,  $V_{FB}$  was negatively shifted and hysteresis decreased. As a result of  $G_p-\omega$  and  $D_{it}$  characteristics, the first  $D_{it}$  was low in 60 min PDA.

In order to reduce the plasma damage of the oxide film deposited using plasma, deposited oxide with pre-oxidation investigated. The combination of PEALD and pre-oxidation through basic dry-oxidation showed superior electrical characteristics to as-deposition oxide. NO oxidation was not to improve the properties much, which seemed to be due to excessive nitridation. However, when pre-oxidation was performed through NO/O<sub>2</sub> mixed gas and N<sub>2</sub>O gas, hysteresis was reduced. Through these experiments, it was found that nitridation less than 0.1% improves the properties.

## Chapter 5. Conclusions

In this dissertation, it was investigated whether the deposition  $\text{SiO}_2$  can be used as the gate oxide of SiC MOS capacitor. To improve characteristics of PEALD and sputtering  $\text{SiO}_2$ , the various PDA and pre-oxidation processes were investigated. Ar and NO PDA were conducted with PEALD  $\text{SiO}_2$ , and  $\text{N}_2$ ,  $\text{NH}_3$ , NO,  $\text{O}_2$  PDA were conducted with sputtering  $\text{SiO}_2$ . The  $\text{O}_2$ , NO, NO/ $\text{O}_2$ , and  $\text{N}_2\text{O}$  pre-oxidation were also investigated to reduce plasma damage on the film during deposition. Electronic properties were characterized with measurements, such as  $C-V$ ,  $J_g-E$ , and the conductance method. Physical and chemical properties were also analyzed by HF etch test, XPS and spectroscopic ellipsometer.

As-deposited PEALD oxides were porous, so PDA should be conducted to densify them. Additional annealing process could be a disadvantage of PEALD compared to simple oxidation process. However, outstanding interface properties of PEALD has already been announced in the literature. The  $1200^\circ\text{C}$  Ar PDA successfully densified the PEALD oxide without deteriorating the interface state. This experiments indicated that PEALD oxide can be used as an insulating film through only densification. Although conventional NO PDA was excessively nitrified due to porous oxide, interface nitridation of ALD oxide film is also possible if annealing conditions are optimized.

Sputtering oxide was also porous like PEALD oxide, and chemically Si-rich film was formed. Therefore, O-containing PDA could effectively complement the oxide film. NO PDA was effective for sputtering oxide because

NO contains N for nitridation and O for re-oxidation. Shorter periods than 2 h were more effective because of its porosity. Through this study, it was confirmed that the sputtering oxide could be used as a MOS gate, which has not been researched sufficiently. However, as-deposition sputtering oxide was imperfect due to Si-rich characteristics. Because of this, a satisfactory breakdown field were not obtained in this experiment. The study of gate oxide using sputtering oxide will still require further experiment.

Pre-oxidation was studied as an alternative of PDA. The PEALD oxide with O<sub>2</sub> pre-oxidation showed insulating properties, which was not shown in PEALD oxide without pre-oxidation. In addition, the nitridation effect of the interface was confirmed by pre-oxidation with NO/O<sub>2</sub> or N<sub>2</sub>O gas. In this results, it was found that the pre-oxidation film protected the plasma damage during deposition, and that the plasma damage affected the interface characteristics. Therefore, if the plasma damage mitigation process is developed, the utilization of the deposition oxide for a gate oxide of MOS device becomes more popular.

The possibility of deposition oxides, PEALD oxide and sputtered oxide, to be used as gate oxide of the SiC MOS devices has been evaluated and proved in this dissertation. Although deposition oxides still remain an optimization step of post annealing to be adopted in a gate oxide of SiC MOS devices, the SiO<sub>2</sub> deposition film, such as PEALD and sputtering, can be used for MOS devices. New processes, pre-oxidation as an alternative of PDA, are also suggested. Since the deposition method is not limited by the substrate material, a new material other than SiO<sub>2</sub> may be used in SiC MOS devices. With further research, the deposition film will be commonly used in SiC devices in near future.



# CURRICULUM VITAE

---

## Suhyeong Lee

Thin Film Research Laboratory

Department of Materials Science and Engineering

College of Engineering, Seoul National University

Gwanak-ro 1, Gwanak-gu, Seoul 08826, Republic of Korea

E-mail: puppls@snu.ac.kr

Tel: +82-10-8772-4378

---

## EDUCATION

**2007.03 – 2011.02**    B.S., Department of Materials Science and Engineering,  
Seoul National University, Seoul, Republic of Korea

**2011.03 – 2018.02**    Ph.D., Department of Materials Science and Engineering,  
Seoul National University, Seoul, Republic of Korea

## **RESEARCH AREAS**

### **1. SiO<sub>2</sub> on 4H-SiC for MOS device application (2013.01 – 2018.02)**

- Understanding gate oxide deposition system for SiO<sub>2</sub>/4H-SiC MOS capacitor
- Research on Atomic Layer Deposition and Sputtering system
- Understanding of post-deposition annealing mechanism
- Fabrication and characterization of 4H-SiC MOS capacitor
- Understanding of SiO<sub>2</sub>/4H-SiC interface from material and electrical properties

### **2. La-silicate on Ge for MOS device application (2011.03 – 2012.12)**

- Understanding atomic layer deposition system for La-silicate/Ge MOS capacitor
- Fabrication and characterization of La-silicate/Ge MOS capacitor
- Understanding of La-silicate/Ge interface system from material and electrical properties

# **TECHNICAL SKILLS**

## **1. Gate dielectric deposition**

- Deposition process of thermal atomic layer deposition
- Deposition process of plasma-enhanced atomic layer deposition
- Deposition process of reactive sputtering

## **2. Oxidation methods**

- Silicon carbide oxidation for gate oxide
- Post-deposition annealing process of furnace

## **3. MOS device fabrication methods**

- Electron-beam evaporation of metals
- Thermal evaporation of metals
- Sputtering of metals
- MA6-II aligner for photo-lithography
- Cleaning and etch process by acid solution

## **4. Electrical properties measurement system**

- Capacitance-voltage measurement by Keithley 4200-SCS
- Capacitance-voltage measurement by HP 4194A and 4284A
- Current-voltage measurement by HP 4155A and Keithley 4200-SCS
- Capacitance-frequency measurement by HP 4194A
- $D_{it}$  extraction from capacitance measurement by conductance method

## **5. Material analysis methods**

- Thickness and refractive index measurement by Spectroscopic Ellipsometer (M-2000, J. A. Woollam)
- Surface topography analysis by Atomic Force Microscopy

(JSPM-5200, JEOL)

– Chemical properties analysis by X-ray Photoelectron Spectroscopy

## **RESEARCH PROJECTS**

2011.03 – 2018.02 / Seoul National University Brain Korea 21 and 21+

(BK21 and BK21+) program of Department of Materials  
Science and Engineering supported by Korea Ministry of  
Education

2011.05 – 2016.02 / Development of terra-bit 3D ReRAM original technology

supported by Korea Ministry of Trade, Industry and  
Energy.

2011.05 – 2013.02 / 3D Development of Integration element process

technology for system semiconductor supported by Korea  
Ministry of Knowledge Economy

2011.08 – 2013.01 / Reliability analysis and modeling of high-k/metal gate

devices supported by Samsung Electronics Inc.

2011.06 – 2012.05 / Development of high efficiency submodule through

optimization of CIGS sputtering process supported by  
Korea Ministry of Knowledge Economy

2011.11 – 2012.10 / Semiconductor in-line CD-SEM with 1.8 nm high

resolution supported by Korea Ministry of Knowledge  
Economy

2012.11 – 2014.01 / Development of Ge and III-V semiconductor process for

high mobility channel devices supported by Samsung  
Electronics Inc.

2013.02 – 2015.02 / Research on fracture characteristics of flexible OLED

encapsulation by optical and electrical technique

supported by Samsung Display Co.

2014.03 – 2015.02 / Development of 3D laminated new device and core

material process technology for next generation memory

supported by Korea Ministry of Trade, Industry and

Energy.

2014.04 – 2016.03 / Development of SiC epitaxy material for energy

semiconductor device supported by Korea Ministry of

Trade, Industry and Energy.

2014.10 – 2016.05 / Development of semi-insulated 8-inch SiC

monocrystalline substrate with resistance of  $10^5$  ohm-cm

for high-temperature/high-frequency devices supported by

Korea Ministry of Trade, Industry and Energy.

## REFERENCES

- [1] J. A. Cooper Jr., "Advances in SiC MOS Technology", *Phys. Status Solidi A* **162**, 305 (1997)
- [2] "www.myseek.org (The site is not available now)" (2016)
- [3] I. Ferain, C.A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors", *Nature* **479**, 310 (2011)
- [4] S.-H. Ryu, A.K. Agarwal, R. Singh, and J.W. Palmour, "1800 V NPN Bipolar Junction Transistors in 4H-SiC", *IEEE Electron Device Lett.* **22**, 124 (2001)
- [5] C.E. Weitzel, J.W. Palmour, J. Calvin H. Carter, and K.J. Nordquist, "4H-SiC MESFET with 2.8 W/mm power density at 1.8 GHz", *IEEE Electron Device Lett.* **15**, 406 (1994)
- [6] S.E. Saddow and A. Agarwal, *Advances in Silicon Carbide Processing and Application* (Artech Houst, Inc., Massachusetts, 2004)
- [7] K. Jarredahl and R.F. Davis, *SiC Materials and Devices* (Academic Press, 1998)
- [8] S. Yoshida, E. Sakuma, H. Okumura, S. Misawa, and K. Endo, "Heteroepitaxial growth of SiC polytypes", *J. Appl. Phys.* **62**, 303 (1987)
- [9] C.J. Glassbrenner and G.A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point", *Phys. Rev.* **134**, A1058 (1964)

- [10] G.L. Harris, *Properties of Silicon Carbide* (INSPEC, the Institution of Electrical Engineers London, United Kingdom, 1995)
- [11] Y. Okada and Y. Tokumaru, "Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500 K", *J. Appl. Phys.* **56**, 314 (1984)
- [12] Z. Li and R.C. Bradt, "Thermal expansion of the hexagonal (6H) polytype of silicon carbide", *J. Am. Ceram. Soc.* **69**, 863 (1986)
- [13] C. Kim, "Improving the interface characteristic of SiO<sub>2</sub>/4H-SiC using nitridation and reduced oxidation process", *Ph.D Dissertation* (Seoul National University, Republic of Korea, 2015)
- [14] R.B. Campbell, "Whatever happened to silicon carbide", *IEEE Trans. Indust. Electron.* **IE-29**, 124 (1982)
- [15] E.O. Johnson, *RCA Rev.* **26**, 163 (1965)
- [16] R.W. Keyes, "Figure of merit for semiconductors for high-speed switches", *Proceedings of the IEEE* **60**, 225 (1972)
- [17] B.J. Baliga, *J. Appl. Phys.* **53**, 1759 (1982)
- [18] M.S. Shur, *SiC Materials and Devices* (Academic Press, 1998), p. 161
- [19] B.J. Baliga, *Advanced Power MOSFET Concepts* (Springer, 2010), p. 23
- [20] J.A. Cooper Jr., M.R. Melloch, R. Singh, A. Agarwal, and J.W. Palmour, *IEEE Trans. Electron Devices* **49**, 658 (2002)
- [21] N.S. Saks and A.K. Agarwal, "Hall mobility and free electron density at the SiC/SiO<sub>2</sub> interface in 4H-SiC", *Appl. Phys. Lett.* **77**, 3281 (2000)
- [22] K. Chatty, S. Banerjee, T.P. Chow, R.J. Gutmann, E. Arnold, and D. Alok, "Hall Measurements of Inversion and Accumulation-Mode 4H-SiC MOSFETs", *Mater. Sci. Forum* **389-393**, 1041 (2002)



- [23] G. Pensl, S. Beljakowa, T. Frank, K. Gao, F. Speck, T. Seyller, L. Ley, F. Ciobanu, V. Afanas'ev, A. Stesmans, T. Kimoto, and A. Schöner, "Alternative techniques to reduce interface traps in n-type 4H-SiC MOS capacitors", *Phys. Status Solidi B* **245**, 1378 (2008)
- [24] P. Deák, J.M. Knaup, T. Hornos, C. Thill, A. Gali, and T. Frauenheim, "The mechanism of defect creation and passivation at the SiC/SiO<sub>2</sub> interface", *J. Phys. D: Appl. Phys.* **40**, 6242 (2007)
- [25] H. Kurimoto, K. Shibata, C. Kimura, H. Aoki, and T. Sugino, "Thermal oxidation temperature dependence of 4H-SiC MOS interface", *Appl. Surf. Sci.* **253**, 2416 (2006)
- [26] X. Shen and S.T. Pantelides, "Identification of a major cause of endemically poor mobilities in SiC/SiO<sub>2</sub> structures", *Appl. Phys. Lett.* **98**, 053507 (2011)
- [27] A. Pérez-Tomás, P. Brosselard, P. Godignon, J. Millán, N. Mestres, M.R. Jennings, J.A. Covington, and P.A. Mawby, "Field-effect mobility temperature modeling of 4H-SiC metal-oxide-semiconductor transistors", *J. Appl. Phys.* **100**, 114508 (2006)
- [28] S.K. Gupta and J. Akhtar, *Thermal Oxidation of Silicon Carbide (SiC) – Experimentally Observed Facts* (INTECH, 2011)
- [29] Y. Song, S. Dhar, L.C. Jeldman, G. Chung, and J.R. Williams, "Modified Deal Grove model for the thermal oxidation of silicon carbide", *J. Appl. Phys.* **95**, 4953 (2004)
- [30] K.L. Luthra, "Some New Perspectives on Oxidation of Silicon Carbide and Silicon Nitride", *J. Am. Ceram. Soc.* **74**, 1095 (1991)
- [31] N.S. Jacobson, "Corrosion of Silicon-Based Ceramics in Combustion

- Environments", J. Am. Ceram. Soc. **76**, 3 (1993)
- [32] V. Šimonka, A. Hössinger, J. Weinbub, and S. Selberherr, "Growth rates of dry thermal oxidation of 4H-silicon carbide", J. Appl. Phys. **120**, 135705 (2016)
- [33] D. Goto, Y. Hijikata, S. Yagi, and H. Yaguchi, "Differences in SiC thermal oxidation process between crystalline surface orientations observed by in-situ spectroscopic ellipsometry", J. Appl. Phys. **117**, 095306 (2015)
- [34] M. Ohring, *Materials Science of Thin Films, 2<sup>nd</sup> edition* (Academic Press, San Diego, 2002) p. 279
- [35] A.R. Barron, "CVD of SiO<sub>2</sub> and related materials: an overview", Adv. Mater. Opt. Electron. **6**, 101 (1996)
- [36] S.-J. Won, "Enhancement of growth rate in atomic layer deposition of dielectric materials", *Ph.D Dissertation* (Seoul National University, Republic of Korea, 2010) p. 10
- [37] V. Bhatt and S. Chandra, "Silicon dioxide films by RF sputtering for microelectronic and MEMS applications", J. Micromech. Microeng. **17**, 1066 (2007)
- [38] M. Farooq and Z.H. Lee, "Optimization of the Sputtering Process for Depositing Composite Thin Films", J. Korean Phys. Soc. **40**, 511 (2002)
- [39] "KERI report", (Issue) Start Page (2004)
- [40] H.-f. Li, S. Dimitrijević, H.B. Harrison, and D. Sweatman, "Interfacial characteristics of N<sub>2</sub>O and NO nitrided SiO<sub>2</sub> grown on SiC by rapid thermal processing", Appl. Phys. Lett. **70**, 2028 (1997)
- [41] G.Y. Chung, J.R. Williams, K. McDonald, and L.C. Feldman, "4H-SiC

- oxynitridation for generation of insulating layers", J. Phys.: Condens. Matter **15**, 1 (2003)
- [42] P. Jamet and S. Dimitrijevic, "Physical properties of N<sub>2</sub>O and NO-nitrided gate oxides grown on 4H SiC", Appl. Phys. Lett. **79**, 323 (2001)
- [43] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, M.D. Ventra, S.T. Pantelides, L.C. Feldman, and R.A. Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide", Appl. Phys. Lett. **76**, 1713 (2000)
- [44] A. Chanthaphan, T. Hosoi, T. Shimura, and H. Watanabe, "Study of SiO<sub>2</sub>/4H-SiC interface nitridation by post-oxidation annealing in pure nitrogen gas", AIP Adv. **5**, 097134 (2015)
- [45] A. Modic, Y.K. Sharma, Y. Xu, G. Liu, A.C. Ahlyi, J.R. Williams, L.C. Feldman, and S. Dhar, "Nitrogen plasma processing of SiO<sub>2</sub>/4H-SiC interfaces", J. Electron. Mater. **43**, 857 (2014)
- [46] Q. Zhu, F. Qin, W. Li, and D. Wang, "Electrical and physical properties of 4H-SiC MOS interface with electron cyclotron resonance microwave nitrogen plasma post-oxidation annealing", Physica B **432**, 89 (2014)
- [47] B. Poobalan, J.H. Moon, S.-C. Kim, S.-J. Joo, W. Bahng, I.H. Kang, N.-K. Kim, and K.Y. Cheong, "Investigation of thermally grown oxide on 4H-SiC by a combination of H<sub>2</sub>O and HNO<sub>3</sub> vapor with varied HNO<sub>3</sub> solution heating temperature", Appl. Surf. Sci. **285P**, 795 (2013)
- [48] S.M. Sze, *Physics of Semiconductor Devices, 2nd edition* (Wiley, New York, 1981)
- [49] T. Hori, *Gate Dielectrics and MOS ULSIs* (Springer-Verlag Berlin Heidelberg, Germany, 1997) p. 23

- [50] A.S. Grove, B.E. Deal, E.H. Snow, and C.T. Sah, Solid-State Electron. **8**, 145 (1965)
- [51] E.H. Nicollian and A. Goetzberger, Appl. Phys. Lett. **7**, 216 (1965)
- [52] D.K. Schroder, *Semiconductor Material and Device Characterization*, 3<sup>rd</sup> edition (John Wiley & Sons, Inc., New York, 2008)
- [53] L.M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes", Solid-state Electron. **5**, 285 (1962)
- [54] C.N. Berglund, "Surface states at steam-grown silicon-silicon dioxide interfaces", IEEE Trans. Electron Dev. **ED-13**, 701 (1966)
- [55] R. Castagné and A. Vapaille, "Apparent interface state density introduced by the spatial fluctuations of surface potential in an MOS stucture", Electron. Lett. **6**, 691 (1971)
- [56] E.H. Nicollian and A. Goetzberger, "The Si-SiO<sub>2</sub> interface-electrical properties as determined by the metal-insulator-silicon conductance technique", Bell Syst. Tech. J. **46**, 1055 (1967)
- [57] M.M. Maranowski and J.A. Cooper Jr., "Time-dependent-dielectric-breakdown measurements of thermal oxides on N-type 6H-SiC", IEEE Trans. Electron Devices **46**, 520 (1999)
- [58] P. Fiorenza, A. Frazzetto, A. Guarnera, M. Saggio, and F. Roccaforte, "Fowler-Nordheim tunneling at SiO<sub>2</sub>/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors", Appl. Phys. Lett. **105**, 142108 (2014)
- [59] K.Y. Cheong, J.H. Moon, H.J. Kim, W. Bahng, and N.-K. Kim, "Current conduction mechanisms in atomic-layer-deposited HfO<sub>2</sub>/nitrided SiO<sub>2</sub>

- stacked gate on 4H silicon carbide", J. Appl. Phys. **103**, 084113 (2008)
- [60] W.-j. Cho and Y.-c. Kim, "Characterization of annealing effects of low temperature chemical vapor deposition oxide films as application of 4H-SiC metal–oxide–semiconductor devices", J. Vac. Sci. Technol., B **20**, 14 (2002)
- [61] G.Y. Chung, J.R. Williams, T. Isaacs-Smith, F. Ren, K. McDonald, and L.C. Feldman, "Nitrogen passivation of deposited oxides on n 4H-SiC", Appl. Phys. Lett. **81**, 4266 (2002)
- [62] A. Pérez-Tomás, P. Godignon, N. Mestres, R. Pérez, and J. Millán, "A study of the influence of the annealing processes and interfaces with deposited SiO<sub>2</sub> from tetra-ethoxy-silane for reducing the thermal budget in the gate definition of 4H–SiC devices", Thin Solid Films **513**, 248 (2006)
- [63] R. Ghandi, B. Buono, M. Domeij, R. Esteve, A. Schöner, J. Han, S. Dimitrijević, S.A. Reshanov, C.-M. Zetterling, and M. Östling, "Surface-passivation effects on the performance of 4H-SiC BJTs", IEEE Trans. Electron Devices **58**, 259 (2011)
- [64] C.S. Hwang, *Atomic Layer Deposition for Semiconductors* (Springer US, 2014)
- [65] C. Kim, J.H. Moon, J.H. Yim, D.H. Lee, J.H. Lee, H.H. Lee, and H.J. Kim, "Comparison of thermal and atomic-layer-deposited oxides on 4H-SiC after post-oxidation annealing in nitric oxide", Appl. Phys. Lett. **100**, 082112 (2012)
- [66] H. Yoshioka, T. Nakamura, and T. Kimoto, "Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures

- using surface potential based on depletion capacitance", J. Appl. Phys. **111**, 014502 (2012)
- [67] A.V. Penumatcha, S. Swandono, and J.A. Cooper, "Limitations of the high-low C-V technique for MOS Interfaces with large time constant dispersion", IEEE Trans. Electron Devices **60**, 923 (2013)
- [68] X. Yang, B. Lee, and V. Misra, "Electrical Characteristics of SiO<sub>2</sub> Deposited by Atomic Layer Deposition on 4H-SiC After Nitrous Oxide Anneal", IEEE Trans. Electron Devices **63**, 2826 (2016)
- [69] S.R. Kodigala, S. Chattopadhyay, C. Overton, I. Ardoin, B.J. Gordon, D. Johnstone, D. Roy, and D. Barone, "Growth and surface analysis of SiO<sub>2</sub> on 4H-SiC for MOS devices", Appl. Surf. Sci. **330**, 465 (2015)
- [70] E. Pitthan, A.L. Gobbi, H.I. Boudinov, and F.C. Stedile, "SiC nitridation by NH<sub>3</sub> annealing and its effects in MOS capacitors with deposited SiO<sub>2</sub> films", J. Electron. Mater. **44**, 2823 (2015)
- [71] Y.-W. Lee, V. Zubkov, M.-Y. Shek, L.-Q. Xia, P. IYENGAR, S. Baluja, S.A. Hendrickson, J.C. Rocha-Alvarez, T. Nowak, and D.R. Witty, "Silicon dioxide layer deposited with BDEAS", (Issue) Start Page (2013)
- [72] L. Huang, B. Han, B. Han, A. Derecskei-Kovacs, M. Xiao, X. Lei, M.L. O'Neill, R.M. Pearlstein, H. Chandra, and H. Cheng, "Density functional theory study on the full ALD process of silicon nitride thin film deposition via BDEAS or BTBAS and NH<sub>3</sub>", Phys. Chem. Chem. Phys. **16**, 18501 (2014)
- [73] S. Dimitrijevic, P. Tanner, and H.B. Harrison, "Slow-trap profiling of NO and N<sub>2</sub>O nitrided oxides grown on Si and SiC substrates",

- Microelectron. Reliab. **39**, 441 (1999)
- [74] H. Yoshioka, T. Nakamura, and T. Kimoto, "Generation of very fast states by nitridation of the SiO<sub>2</sub>/SiC interface", J. Appl. Phys. **112**, 024520 (2012)
- [75] C.C. Chang, "Auger electron spectroscopy", Surf. Sci. **25**, 53 (1971)
- [76] S. Lee, Y.S. Kim, H.J. Kang, H. Kim, M.-W. Ha, and H.J. Kim, "Effects of post-deposition annealing on sputtered SiO<sub>2</sub>/4H-SiC metal-oxide-semiconductor", Solid State Electronics **139**, 115 (2018)
- [77] T. Ito, T. Nozaki, and H. Ishikawa, "Direct thermal nitridation of silicon dioxide films in anhydrous ammonia gas", J. Electrochem. Soc.: Solid-state Sci. Technol. **127**, 2053 (1980)
- [78] B.V. Crist, *Handbook of the elements and native oxides* (XPS International, Inc., 1999)
- [79] J.F. Moulder, W.F. Stickle, P.E. Sobol, and K.D. Bomben, *Handbook of X-ray photoelectron spectroscopy* (Perkin-Elmer Co., 1992)
- [80] E.H. Nicollian and J.R. Brews, *MOS (metal oxide semiconductor) physics and technology* (Wiley-Interscience Publication, New Jersey, 1982)
- [81] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices", Jpn. J. Appl. Phys. **54**, 040103 (2015)
- [82] A.G. Shard, "Detection limits in XPS for more than 6000 binary systems using Al and Mg K $\alpha$  X-rays", Surf. Interface Anal. **46**, 175 (2014)

# LIST OF PUBLICATIONS

## 1. International Journals

- [1] Suhyeong Lee, Young Seok Kim, Hong Jeon Kang, Hyunwoo Kim, Min-Woo Ha, and Hyeong Joon Kim, “Effects of post-deposition annealing on sputtered SiO<sub>2</sub>/4H-SiC metal-oxide-semiconductor”, Solid State Electronics **139**, 115 (2018)
- [2] Hong Jeon Kang, Jeong Hyun Moon, Wook Bahng, Suhyeong Lee, Hyunwoo Kim, Sang-Mo Koo, Dohyun Lee, Dongwha Lee, Hoon-Young Cho, Jaeyeong Heo, and Hyeong Joon Kim, “Oxygen- and photoresist-related interface states of 4H-SiC Schottky diode observed by deep-level transient spectroscopy”, Journal of Applied Physics **122**, 094504 (2017)
- [3] Hyunwoo Kim, Hunhee Lee, Young Seok Kim, Suhyeong Lee, Hongjeon Kang, Jaeyoung Heo, and Hyeong Joon Kim, “On-axis Si-face 4H-SiC epitaxial growth with enhanced polytype stability by controlling micro-steps during the H<sub>2</sub> etching process”, CrystEngComm **19**, 2359 (2017)
- [4] Changhyun Kim, Suhyeong Lee, Jeong Hyun Moon, Joon Rae Kim, Hunhee Lee, Hongjeon Kang, Hyunwoo Kim, Jaeyeong Heo, and



Hyeong Joon Kim, “The effect of reduced oxidation process using ammonia annealing and deposited oxides on 4H-SiC metal-oxide-semiconductor structure”, ECS Solid State Letters **4**, N9 (2015)

[5] Hunhee Lee, Hyunwoo Kim, Han Seok Seo, Dohyun Lee, Changhyun Kim, **Suhyeong Lee**, Hongjeon Kang, Jaeyeong Heo, and Hyeong Joon Kim, “Comparative study of 4H-SiC epitaxial layers grown on 4° off-axis Si- and C-face substrates using bistrimethylsilylmethane precursor”, ECS Journal of Solid State Science and Technology **4**, N89 (2015)

[6] Yu Jin Choi, Hajin Lim, **Suhyeong Lee**, Sungin Suh, Joon Rae Kim, Hyung-Suk Jung, Sanghyun Park, Jong Ho Lee, Seong Gyeong Kim, Cheol Seong Hwang, and Hyeong Joon Kim, “Improving the electrical properties of lanthanum silicate films on Ge metal oxide semiconductor capacitors by adopting interfacial barrier and capping layers” ACS Applied Materials & Interfaces **6**, 7885 (2014)

[7] Dohyun Lee, Changhyun Kim, Hunhee Lee, **Suhyeong Lee**, Hongjeon Kang, Hyunwoo Kim, Hui Kyung Park, Jaeyeong Heo, and Hyeong Joon Kim, “Improving the Barrier Height Uniformity of 4H-SiC Schottky Barrier Diodes by Nitric Oxide Post-Oxidation Annealing”, IEEE Electron Device Letters **35**, 868 (2014)

## 2. Domestic Journals

- [1] 이수형, 김형준, "원자층 증착법(ALD)을 이용한 SiC MOS 게이트 산화막의 형성, 한국전기전자재료학회 [E<sup>2</sup>M] 전기 전자와 첨단 소재 **30** (2017)

## 3. International Conferences

- [1] Hong-Jeon Kang, Suhyeong Lee, Hyunwoo Kim, Sungmin Kim, Seongkyung Kim, Wook Bahng, Jeong Hyun Moon, Dohyun Lee and Hyeong Joon Kim, "Minority carrier traps in n-type 4H-SiC measured by Schottky diode-based deep level transient spectroscopy", 11th European Conference on Silicon Carbide and Related Materials (ECSCRM 2016), 25 – 29 September 2016, Halkidiki, Greece
- [2] Hyunwoo Kim, Hunhee Lee, Suhyeong Lee, Hong Jeon Kang, Young Seok Kim and Hyeong Joon Kim, "Enhancing polytype stability of 4H-SiC homoepitaxial growth on on-axis substrates by controlling micro-steps", 11th European Conference on Silicon Carbide and Related Materials (ECSCRM 2016), 25 – 29 September 2016, Halkidiki, Greece
- [3] Changhyun Kim, Suhyeong Lee, Hunhee Lee, Hyunwoo Kim, Hong Jeon

Kang, and Hyeong Joon Kim, “Enhancement of SiO<sub>2</sub>/4H-SiC interface properties using ALD oxides and nitridation”, Pacsurf 2014, 7 – 11 December 2014, Hawaii, USA

[4] Hunhee Lee, Dohyun Lee, Changhyun Kim, Hyunwoo Kim, Suhyeong Lee, Hongjeon Kang, and Hyeong Joon Kim, “Comparative study of 4H-SiC epitaxial layers grown on 4° off-axis Si- and C-face substrates using BTMSM”, 10th European Conference on Silicon Carbide and Related Materials (ECSCRM 2014), 21 – 25 September 2014, Grenoble, France

[5] Dohyun Lee, Changhyun Kim, Hunhee Lee, Suhyeong Lee, Hongjeon Kang, Hyunwoo Kim, Jeong Hyun Moon, and Hyeong Joon Kim, “Improving uniformity of Schottky barrier height of 4H-SiC Schottky barrier diode by nitride sacrificial oxidation”, The International Conference on Silicon Carbide and Related Materials (ICSCRM 2013), 29 September – 4 October 2013, Miyazaki, Japan

#### 4. Domestic Conferences

[1] 강홍전, 이수형, 김현우, 김성민, 김성경, 방욱, 문정현, 이도현, 김형준, “4H-SiC의 슷키접합 다이오드구조 기반 깊은 준위 일시적 검출기 (DLTS)를 이용한 소수운반체 트랩의 관찰”, 2016년 한국세라믹학회 추계학술대회 및 총회, 2016년 11월 23일 – 25일, COEX, 서울

- [2] 이수형, 김준래, 김현우, 강홍전, 김영석, 김형준, "4H-SiC 기판 위에 원자층 증착법으로 증착한 게이트 산화막의 일산화질소 열처리 위치에 따른 전기적 특성", 2016년 한국세라믹학회 춘계학술대회 및 총회, 2016년 4월 20일 - 22일, BEXCO, 부산
- [3] 김현우, 이훈희, 이수형, 강홍전, 김형준, "BTMSM 전구체를 이용한 온액시스 탄화규소 기판 위의 에피택시 성장", 2015년 한국세라믹학회 추계학술대회 및 총회, 2015년 11월 4일 - 6일, 송도컨벤시아, 인천
- [4] 강홍전, 김현우, 이수형, 김형준, "Deep level transient spectroscopy로 측정한 4H-SiC 단결정의 point defects의 energy levels과 density", 2015년 한국세라믹학회 추계학술대회 및 총회, 2015년 11월 4일 - 6일, 송도컨벤시아, 인천
- [5] 이수형, 김준래, 김창현, 이훈희, 김현우, 강홍전, 김형준, "4H-SiC의 표면을 건식산화와 일산화질소 산화로 처리한 원자층 증착 산화막의 전기적 특성", 2015년 한국세라믹학회 춘계학술대회 및 총회, 알펜시아리조트, 2015년 4월 15일 - 17일, 알펜시아 리조트, 평창
- [6] 최유진, 임하진, 이수형, 서성인, 김준래, 박상현, 김형준, "Ge 기판을 이용한 원자층증착법을 통한 La-silicate 막의 전기적 특성", 한국반도체디스플레이기술학회 2013년 추계학술대회 및 제 4회 반도체공정포럼 반도체차세대 공정장비기술 심포지엄, 2013년 10월 23일, 한국

- [7] 김창현, 이수형, 이도현, 이훈희, 김현우, 김형준, "원자층증착산화막의 적층과 암모니아 열처리를 이용한  $\text{SiO}_2/4\text{H-SiC}$  계면에서의 재산화 방지 및 절연특성의 향상 방법", 한국반도체디스플레이기술학회 2013년 추계학술대회 및 제 4회 반도체공정포럼 반도체차세대 공정 장비기술 심포지엄, 2013년 10월 23일, 한국반도체산업협회, 성남
- [8] 이훈희, 이도현, 김창현, 김현우, 이수형, 강홍전, 김성경, 김형준, "4° off-axis 4H-SiC 기판에서의 스텝번칭이 발생하지 않는 Homoepitaxy 성장 연구", 2013년 한국세라믹학회 추계총회 및 연구발표회, 2013년 10월 16일 - 18일, 제주국제컨벤션센터, 제주
- [9] 이도현, 김창현, 이훈희, 이수형, 강홍전, 김현우, 김형준, "NO 열처리를 통한 4H-SiC 쇼트키 다이오드의 쇼트키 장벽 균일도와 항복전압 향상", 2013년 한국세라믹학회 추계총회 및 연구발표회, 2013년 10월 16일 - 18일, 제주국제컨벤션센터, 제주
- [10] 김창현, 이수형, 이도현, 이훈희, 김현우, 강홍전, 김형준, "원자층 증착 산화막의 적층과 암모니아 열처리를 이용한  $\text{SiO}_2/4\text{H-SiC}$  계면의 재산화 방지 및 절연파괴 특성의 향상방법", 2013년 한국세라믹학회 추계총회 및 연구발표회, 2013년 10월 16일 - 18일, 제주국제컨벤션센터, 제주
- [11] 이훈희, 김현우, 이도현, 김창현, 이수형, 강홍전, 김형준, "BTMSM소스

를 이용한 on-axis 기판에서의 6H-SiC 동종 단결정 박막 성장에 관한 연구", 한국반도체디스플레이기술학회 2013년 춘계학술대회 및 제 1회 SiC 전력반도체 심포지움, 2013년 5월 31일, 한국교원단체총연합회관, 서울

[12] 이수형, 임하진, 최유진, 양봉섭, 오승하, 김형준, "표면 처리를 통한 LaSiO/Ge MOS capacitor의 전기적 특성 평가", 한국반도체디스플레이기술학회 2013년 춘계학술대회 및 제 1회 SiC 전력반도체 심포지움, 2013년 5월 31일, 한국교원단체총연합회관, 서울

[13] 김현우, 이훈희, 이도현, 김창현, 이수형, 강홍전, 김형준, "KOH 에칭을 이용한 4H-SiC 단결정 박막의 표면결함 분석" 한국반도체디스플레이기술학회 2013년 춘계학술대회 및 제 1회 SiC 전력반도체 심포지움, 2013년 5월 31일, 한국교원단체총연합회관, 서울

[14] 김창현, 이도현, 이수형, 이훈희, 김현우, 김형준, "재산화 방지를 위한 원자층 증착 산화막과 암모니아 열처리가 SiO<sub>2</sub>/4H-SiC에 미치는 영향" 한국반도체디스플레이기술학회 2013년 춘계학술대회 및 제 1회 SiC 전력반도체 심포지움, 2013년 5월 31일, 한국교원단체총연합회관, 서울

[15] 임하진, 최유진, 이수형, 구자흠, 이내인, 김형준, "GaAs를 이용한 고유전율 게이트 산화막 특성 평가", 한국반도체디스플레이기술학회 2012년 추계학술대회, 2012년 10월 10일, KINTEX, 일산

[16] 이수형, 최유진, 임하진, 김준래, 양봉섭, 김형준, "NH<sub>3</sub> 플라즈마 표면 처리를 통한 Ge MOS capacitor의 전기적 특성 평가", 한국반도체디스플레이기술학회 2012년 추계학술대회, 2012년 10월 10일, KINTEX, 일산

[17] 임하진, 이수형, 최유진, 정형석, 원석준, 구자흠, 이내인, 김형준, "The effects of interface and bulk trap of HfO<sub>2</sub> on BTI characteristics", 한국반도체디스플레이기술학회 2012년 춘계학술대회 및 제 2회 반디제주포럼, 2012년 5월 18일, 제주대학교 국제교류회관, 제주

## 국문 초록

Silicon carbide (SiC)는 silicon (Si)보다 높은 녹는점, 높은 파괴 전압 및 밴드 갭을 가지고 있는 물질이다. 이러한 SiC의 특징은 SiC가 고온, 고주파 고전압의 환경에서 사용되는 전력 반도체의 기본 재료로 이용될 수 있도록 만들어 준다. 4H-SiC에 제작된 metal-oxide-semiconductor field effect transistor (MOSFET)은 전력 반도체에서 중요한 역할을 할 것으로 기대되고 있다. 그러나, 산화 과정에서 발생하는 탄소 클러스터들이 interface state를 형성하여 소자 성능을 열화시키는 문제가 존재한다. 이를 해결하기 위해, 많은 연구에서 산화질소 (NO) 가스를 이용한 post-oxidation annealing (POA) 공정을 연구하였으며, 이는 효과적으로 interface state를 제거하였다. 그러나 비록 NO POA가 효과적이더라도, 근본적으로 interface state를 제거하는 방법의 연구가 필요하다. 증착은 이러한 방법 중 하나이다. Chemical vapor deposition (CVD)와 atomic layer deposition (ALD)로 게이트 산화막을 증착하는 연구는 꾸준히 진행되어 왔다. 특히 ALD와 NO post-deposition annealing (PDA)를 이용하였을 때, MOSFET의 성능을 향상시킬 수 있음이 보고 되어있다. 다만 이러한 결과는 30 nm 이하의 산화막 두께에 대한 결과로, 상업적으로 이용되는 산화막은 50 nm 이상이므로 보완이 필요하다. 이 학위논문에서는 40 nm 혹은 그 이상의 산화막 두께를 plasma enhanced ALD (PEALD)와 sputtering으로 증착하고, capacitor를 형성하여 전기적 성질 및 물리적, 화학적 성질을 분석하였다. 또한 증착막에 대해서 PDA 조건을 조사하였다. 덧붙여 PDA를 사용하지 않는 증착막의 활용을 위해 열산화막으로 버퍼층을 형성한 뒤 증착한 산화막을



평가하였다.

50 nm의 두께로 증착한 PEALD  $\text{SiO}_2$  산화막을 외부 반응이 없이 열에너지로 고밀도화가 가능한 지 평가하기 위하여 Ar을 이용하여 PDA를 진행하였다. Ar PDA는 400, 600, 800, 1000, 1200° C 의 온도에서 2시간 동안 진행되었다. HF 식각 테스트와 누설 전류 분석을 통해 산화막이 1000° C 이상의 온도에서 안정화 되었음을 알아내었다. 그러나,  $C-V$  분석에서는 1200도의 온도에서 안정화 됨을 파악하였다. 추가적으로 NO PDA를 통한 열처리에서는  $C-V$  hysteresis가 열처리를 하지 않은 산화막에 비해 크게 감소하였지만, flat-band 전압 ( $V_{FB}$ ) 가 음의 값을 가졌다. 이는 과도한 질화처리로 인해 산화막 혹은 계면에 양의 전하로 차징이 된 것으로 보인다.

한편, sputtering은 전통적인 physical vapor deposition (PVD) 증착 방식이지만, 게이트 산화막의 증착에는 주로 이용되지 않았다. Sputtering  $\text{SiO}_2$  산화막이 절연막으로 이용 될 수 있는지를 평가하기 위하여, reactive sputtering으로 증착한  $\text{SiO}_2$  산화막을 이용하여 MOS capacitor를 제작하여 평가하였다. 산화막은  $\text{N}_2$ ,  $\text{NH}_3$ ,  $\text{O}_2$ , NO PDA를 통해 변화를 관찰하였고, 전기적 성질과 물리적 성질을 분석하였다. 열처리 된 모든 샘플들은 굴절률과 HF 식각 테스트를 통해 충분히 고밀도화 되었음을 파악하였다. 그러나  $\text{N}_2$ 와  $\text{NH}_3$  PDA를 거쳤을 때는 절연 특성을 보이지 않았으며, 이는 nitrogen 반응에 의한 결과로 보인다.  $\text{O}_2$ 와 NO PDA에서는 산소와의 반응으로 절연 특성을 나타내었지만, 열산화막보다 뒤떨어지는 특성을 보였다.  $C-V$  결과에서 NO PDA 시 많은 양의 양전하가 산화막에 침투되었음이 파악되었다. NO PDA의 최적화를 위해 30, 60, 90분의 조건으로 열처리를 하여 평가하였다. PDA 시간이

증가할수록,  $V_{FB}$ 는 음의 방향으로 이동하였으며, hysteresis는 감소하였다.

Interface state는 세 조건 중 60분에서 가장 낮은 값을 보였다.

PEALD와 sputtering은 모두 플라즈마를 이용하며, 플라즈마 데미지가 기판에 미치는 영향을 파악할 필요가 있다. 이를 위해 pre-oxidation을 통해 산화막을 증착 전 얇게 형성하여 플라즈마에서 기판을 보호한 뒤 분석하였다. 기존의 PDA를 하지 않은 박막은 절연 특성이 형편없었지만, pre-oxidation을 거친 뒤 증착한 박막은 PDA를 하지 않고도 절연 특성을 나타내었으며 누설전류가 크게 감소하였고, 정상적인  $C-V$  곡선을 얻을 수 있었다. 비록 누설 전류가 열산화막에 만큼 우수한 것은 아니지만, 전체적으로 PEALD와 sputtering oxide를 향상시켰다. 이러한 결과를 바탕으로, NO와  $N_2O$ 를 이용해서 pre-oxidation을 진행하였다. 이 때,  $N_2O$ 와 NO/ $O_2$  혼합 가스를 이용했을 때 뛰어난  $C-V$  특성을 보이는 박막이 형성되었다.

이 학위논문에서는 증착  $SiO_2$ 가 게이트 산화막으로 이용될 수 있는지를 평가하였다. PEALD와 sputtering  $SiO_2$ 의 특성을 향상시키기 위해 PDA와 pre-oxidation을 진행하였고, 다양한 조건에서 평가하여 실제로 PEALD와 sputtering 산화막이 게이트 절연막으로 사용될 수 있음을 보였다. 다만 누설 전류 특성이 아직 열산화막에 뒤떨어진다. 만약 증착과 열처리 조건을 최적화한다면, 증착 산화막이 4H-SiC의 MOS 소자의 게이트 산화막으로 이용되기에 충분한 경쟁력을 갖출 것이다.

---

주요어 : 4H-SiC, MOS capacitor, PEALD, sputtering, post-deposition annealing

학 번 : 2011-20658